GenRad

SERVICE MANUAL

2511/2514

VIBRATION CONTROL SYSTEMS

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PATENTS

U.S.	3,710,082
	3,848,115
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West Germany	2,220,416
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REVISION RECORD

Released per PRB #3210, September 1983

Revision 2, per ECN 2777, September 1983

Revision 2 of the 2511 Service Manual reflects the addition of the following options: (1) the LSI-11/23 controller, (2) rack and pedestal mounting, (3) Winchester disk drive, to the 2511 system. Revision 2 also introduced the 2514 configuration which consists of a basic 2511 unit which includes the optional 64K memory, LSI-11/23 and Winchester disk drive as standard items.

Revision 2, Change 1, per ECN 2986, June 1986

Change 1 reflects inclusion of Revision 2 Backplane modification, and Q-bus protocol information.

Revision 2, Change 2, per ECN 2986, July 1986

Change 2 reflects additional information regarding backplane modification, Q-bus protocol, and miscellaneous editing.

FOREWORD

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> During the first ninety (90) days after originial installation, on-site at no charge unless such service is specifically excluded in the terms and conditions of sale.

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SERVICE POLICY

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>
> By GenRad on a per call basis with no contract, or
>
> By the customer, after purchase of spares and service training from GenRad.

GenRad policy is to maintain product repair capability for a period of five (5) years after original installation.

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CHAPTER 1

INTRODUCTION

1.1 SCOPE AND ORGANIZATION

GenRad service publications for the 2511/2514 Vibration Control Systems (VCS) are supplied in the following volumes:

2511/2514 Service Manual	2511-0101
2511/2514 System Reference Manual	2511-0102
2511/2514 System Diagnostic Manual	2511-0690

These manuals are intended for use by qualified service technicians who have attended the GenRad 2511/2514 service training course and the prerequisite Digital Equipment Corporation training on the PDP-11/LSI-11 computer (or equivalent experience). The user is assumed to be familiar with LSI-11 and PDP-11 Unibus operation, peripheral interfaces, and with general digital circuitry.

This basic Service Manual volume (2511-0101) contains theory of operation for the GenRad manufactured hardware components, general service information, and calibration and alignment procedures that are used in conjunction with some of the diagnostic software programs. Service of the 2511/2514 depends primarily on the use of the diagnostic software. This manual provides background information on the 2511/2514 units and circuits to aid in understanding and effective use of the diagnostics.

The System Reference volume (2511-0102) contains the assembly drawings and detailed schematics that are referenced herein. They are bound separately for convenience of reference and maintenance revisions.

The System Diagnostic volume (2511-0690) provides descriptions of the diagnostic programs, instructions for their operation, and troubleshooting hints to aid in detection of problems and isolation so far as possible to a particular unit or circuit board. Maintenance is based on replacement of defective boards or units. In some cases, problems may be traced to chip level, but that is generally not practical and field repair of boards is not recommended. The Diagnostic manual corresponds to a software package and is maintained separately so it can be easily revised for software changes. The diagnostic programs exercise and test both GenRad and vendor units in the system. Hardware manuals for the vendor components are supplied with the system or the required training courses.

1.2 EQUIPMENT RETURN

Before returning any equipment to GenRad for service, obtain a "Returned Material" (RM) number from the nearest GenRad office. Use of this number in all correspondence and on a tag tied to the returned item will ensure proper handling and identification. For equipment not covered by warranty, a purchase order should be forwarded to avoid unnecessary delay.

For return shipment, use the original packing, shipping cases, or packaging that will protect the unit from damage during transit. Advice may be obtained from the nearest GenRad office.

1.3 SPECIFICATIONS

Table 1-1 lists the specifications for the 2511/2514 Systems.

1.4 ACCESSORIES AND OPTIONS

Table 1-2 lists the accessories and options available for the 2511/2514 Systems at the time of printing.

Table 1-1. Features, Characteristics, and Specifications

Characteristics	Specification			
SYSTEM SIZE AND WEIGHT	Width	Depth	Height	Weight
Keyboard:	18 in (45.7 cm)	7.5 in (19 cm)	1.5 in 3.8 cm)	nominal 33 lbs (14.9 Kg)
CRT:	18 in (45.7 cm)	12.5 in (31.8 cm)	12. in (30.5 cm)	
Disk Enclosure:	5.9 in (15 cm)	3.4 in (9 cm)	8.3 in (21 cm)	8.2 lbs (3.75 Kg)
VCS Box:	19.7 in (50 cm)	11.5 in (29 cm)	26 in (66 cm)	85 lbs (38.5 Kg)
SYSTEM POWER REQUIREMENTS				
Service:	Single-phase, 3 wire, 30 A			
Power:	850 watts 115 V, aproximately 15 A 230 V, approximately 6 A			
Frequency:	60 Hz 50 Hz			
SYSTEM ENVIRONMENT				
Temperature:	10 to 50 deg C (50 to 122 deg F)			
Humidity:	8 to 80 percent, non-condensing			
Maximum Thermal Gradient:	15 deg F per hour.			
ANALOG INPUT SPECIFICATIONS				
Input:	Single-ended (BNC connectors) 10 ohm to system ground low side return			
Number of Input Channels:	One standard on 2511, two standard on 2514, up to four optional			
Maximum Input Frequency Range:	DC to 25 kHz with anti-alias protection on all channels			
Impedance:	1M ohm shunted by < 100 pf			

Table 1-1. Features, Characteristics, and Specifications (Continued)

Characteristics	Specification
Full Scale (FS) Ranges:	.125, .25, .5, 1.0, 2.0, 4.0, 8.0, 10.0 V peak
Auto Ranging:	Selectable for all channels
Gain Accuracy:	±.5%
Max Input (operating):	±10 V (protected to ±30 V)
Input Coupling:	dc or ac (-3 dB at 1 Hz)
DC Offset:	Auto zeroing to ±.5% FS
Harmonic Distortion:	<.1% (60 dB down from FS) - on 1 volt or less FS ranges
Crosstalk Between Channels:	>60 dB isolation between channels with input signals that are within selected input ranges
Overall Noise Level:	>60 dB down all ranges
Overload Detection:	On converted (digital) value
Throughput (at 2.56:1 oversampling):	Max bandwidth: 25 kHz; Number of channels: 4 or less
ANTI-ALIAS FILTERS	
Type:	Cascaded 6 pole Chebyshevs
Cutoff Frequencies (f_c):	75 selectable cutoff frequencies for each CH.
Alias Protection:	>70 dB down with 2.56:1 oversampling
Filter Ripple:	±.5dB, 0 to .9 f_c
Phase Matching:	±5° between channels 0 to .9 f_c ±10° @ f_c
Attenuation at f_c:	-1 dB
Cutoff Frequency Accuracy:	-1%, +.5%
Rolloff:	72 dB/octave
SAMPLING	
Modes:	Internal or external
External Clock Input:	TTL level, "0" true, 100 ns min pulse duration
Internal Rates:	$fs = \frac{clock}{nx10^k}$, clock = 4.0 MHz "time" / 4.096 MHz "freq"; k = 0, 1, 2; n = 1,2,3, . . . 4095, 4096
Max Sampling Rate:	$fs\ max = \frac{10^6}{4.1\ \mu s + L \times 2.9\ \mu s}$; L = number of channels being utilized
Multichannel sampling interval:	Simultaneous sampling on all channels
Acquisition Time:	4-5 μs simultaneous on all channels
Aperture Uncertainty:	±5 ns

Table 1-1. Features, Characteristics, and Specifications (Continued)

Characteristics	Specification
CONVERSION CHARACTERISTICS	
Number of Bits:	12
Conversion Time:	2 μs + .9 μs +multiplexer setting
Data Output Mode:	Direct memory access (DMA) transfer
Buffering:	Automatic double buffering for up to eight channels (4 max in 2511)
Demultiplexing:	Automatic into n buffers (2n for double buffering) when n is the number of channels being sampled
Frame Size per Channel:	128 to 16K in a binary sequence. Frame size doubles for zero insertion.
TRIGGER	
Source:	Channel 1, 2, 3 external, digital or free run
Slope/Threshold:	+,- slope, -FS to +FS in 64 steps
External Input:	±2 volt range, dc coupled
Threshold Accuracy:	±5% FS
Transient Capture Delay:	Up to 2K
DIGITAL OUTPUT SPECIFICATIONS	
Number of Output Channels:	One
Output Impedance:	50 ohms
Digital to Analog Converter:	12-bit resolution, ±10 volt maximum output.
SPECTRAL RESOLUTION	Selectable for 100, 200, 400, or 800 lines with standard application package; up to 3200 lines (standard on 2514) with additional memory.
DATA STORAGE	Total capacity, 0.5 M bytes per diskette. 20 megabytes for the Winchester (standard on 2514).

CHAPTER 2

INSTALLATION AND CHECKOUT

This section describes the site requirements for the 2511/2514 systems and provides additional general reference information for the hardware configuration and unit interconnects.

2.1 INSTALLATION POLICY

Initial installation and checkout at the customer facility is included in purchase and warranty conditions. Upon notification of receipt, GenRad Service personnel will come to the site, unpack and inspect the equipment, install and connect all units, and thoroughly check calibration and operation with diagnostic test programs and demonstrations of the operating software.

WARNING

These installation notes are for qualified Service personnel only. Removal of covers may expose lethal shock hazards, particularly if ac power distribution has been damaged or disturbed. Also, operation of the system before initial installation by GenRad personnel could aggravate possible damage to the equipment and may void the warranty.

If there is any evident damage to the shipping containers, the carrier's agent should be notified and requested to be present for unpacking.

2.2 DIMENSIONS AND WEIGHT

The 2511/2514 systems are intended for mounting on a sturdy bench, table, or desk. Total weight of all units is approximately 130 lbs (58.5 kg). Overall dimensions and weight of the major units are listed in Table 1-1.

2.3 POWER

The 2511/2514 systems must be ordered for 115 or 230 VAC nominal, 50 or 60 Hz. Field conversion of voltage or frequency is not practical. All units together, including the optional printer, draw 850 watts. The main power cord has either a 3-conductor grounding plug for 115 V service 15 A (4203-0012) or a 3-conductor grounding plug for 250 V service 6 A (4200-0280).

WARNING

The 3-conductor grounding power cord of the 2511/2514 must be connected only to a properly grounded service receptacle.

External grounding, other than through the main power cord and power cords to the other units, is not required for this equipment. However, if desired, an external chassis ground is available and labeled on the rear of the panel.

For European installation, the American/Canadian standard 250 V plug must be replaced locally. The color code conversion is as follows:

Conductor	North American	European
Neutral	White	Light Blue
Live (Phase)	Black	Brown
Earth Green	Yellow/Green	

2.4 ENVIRONMENT

While the 2511/2514 systems do not require a special environment, reasonable cleanliness and freedom from excessive dust are always necessary, particularly for the disk drive. Ideally, the equipment should be located in a typical computer room environment with cool, filter, humidified air supply maintained at higher pressure than adjacent areas to minimize dust infiltration. The minimum requirements for the 2511/2514 systems as a whole are listed in Table 1-1.

2.5 RECEIVING INSTRUCTIONS

Check the shipment received against the packing list to ensure that the correct number of cartons have been received, and that they are the correct ones. If the correct number of cartons have not been delivered, notify the customer and STP Product Service of the discrepancies.

If the customer did not purchase insurance, they should check with the carrier to locate the missing carton(s) and have the missing carton(s) delivered to the site. If the terms and conditions of the sale are F.O.B. destination, have the Branch Field Service manager or Branch Supervisor check with STP traffic and shipping to locate the missing carton(s). If a carton is lost in transit and cannot be located by the carrier, call STP Product Service.

2.6 UNPACKING AND INSPECTION

If there is any evident damage to shipping cartons, the carriers agent should be present for unpacking. If any of the cartons have been damaged or opened, call it to the attention of the customer and document it on the Field Service Report (FSR).

NOTE

If possible, photographs should be taken of the damaged carton(s) to assist the adjuster in clarifying and determining the extent of damage when filing damage claims. If the damage is extensive, call the Branch Field Manager immediately to report the damage and to get further instructions.

All shipping cartons should be moved to the installation site by the customer. Open each carton, one at a time, and inventory the contents of each against the packing list. If any item is missing or damaged, inform the customer and note it on the FSR.

NOTE

Ensure that any missing items are not covered by a special waiver or is an approved partial shipment.

Remove the shipping restraints from within the system box. Their locations will be evident by inspection and removal is straightforward. Inspect both backplanes for bent pins, wires or foreign material. Also, check between modules for any hardware or foreign material that may be lodged between them.

2.7 INTERNAL AND PERIPHERAL INTERCONNECT CABLING

Figure 2-1 shows the normal locations of all circuit boards in the system box and the signal interconnection cabling between them and the other units.

Three slot configurations are available for Revisions 1 and 2 backplanes depending on the number of options (none, one, or two) in the system.

Revision 1 backplane consists of two slot configurations using either a short or long Q-Bus to Unibus cable. The configurations differ in slots 1 through 4 as shown below.

Revision 1 Backplane, P/N 2511-2010/1
(Long Q-U Cable)

	A	B	C	D	E	F
1	(1) SPARE		(2) SPARE		(3) LSI-11 CONTROLLER	
2	(6)		(3) Q - D A S		(4)	
3	(7) DISK CONTROLLER		(8) MEMORY		(9) Q-BUS INTERFACE	
4	PADDLEBOARD		UNUSED		UNUSED	

( ) = Q-Bus Protocol

Revision 1 Backplane, P/N 2511-2010/1
(Short Q-U Cable)

	A	B	C	D	E	F
1	(1) SPARE		(2) SPARE		(3) LSI-11 CONTROLLER	
2	(6)		(3) Q - D A S		(4)	
3	(7) Q-BUS INTERFACE		(8) DISK CONTROLLER		(9) MEMORY	
4	PADDLEBOARD		UNUSED		UNUSED	

( ) = Q-Bus Protocol

Revision 2 backplane configuration differs in slots 1 through 4 also and is shown below.

Revision 2 Backplane, P/N 2511-2010/2

	A	B	C	D	E	F
1	(7) MEMORY		(6) DISK CONTROLLER		(1) SPARE	
2	(8)		(5) Q - D A S		(2)	
3	(9) Q-BUS INTERFACE		(4) LSI-11 CONTROLLER		(3) SPARE	
4	PADDLEBOARD		(10) TERMINATOR			

( ) = Q-Bus Protocol

Systems with Revision 2 backplanes (part number 2511-2010/2) are minimally connected as shown in Figure 2-2.

Table 2-1 lists the Revision 2 board locations for a system with no options, one option, and two options (loaded).

Table 2-1. Revision 2 Slot Configurations

Slot	Bus Position	No Options	1 Option	2 Options
4CD	10	Terminator	Terminator	Terminator
3AB	9	Q-Bus Interface	Q-Bus Interface	Q-Bus Interface
2AB	8	Q-DAS	Q-DAS	Q-DAS
1AB	7	Memory	Memory	Memory
1CD	6	Disk Controller	Option	Option
2CD	5	Q-DAS	Q-DAS	Q-DAS
3CD	4	LSI-11 Controller	Disk Controller	Option
3EF	3	Spare	LSI-11 Controller	Disk Controller
2EF	2	Q-DAS	Q-DAS	Q-DAS
1EF	1	Spare	Spare	LSI-CPU

CAUTIONS

- The Q-DAS board (2511-4701) can only be mounted on the 2511 backplane in slot 2. If the Q-DAS is mounted any where else in the system, it may cause severe damage to the system.

- Many of the connectors on the multi-conductor ribbon cables are not mechanically keyed to prevent reversed installation. All of them, however, have some kind of visible marking to indicate proper mating; for example, small diamond shaped markers, or pin numbering indications. If there is any question about proper orientation, examine the connectors very carefully to verify that they are properly mated.

- The LSI-11 Controller can NOT be mounted in slot two. The ± 15 volt supply wire here for the Q-DAS board will damage the controller.

Check the seating of the circuit boards and the signal interconnect cabling. The disk drive, keyboard, and printer have captive signal cables, all of which are connected to plainly marked receptacles at the rear of the system box. The display unit is driven by a video signal supplied through a separate BNC-to-BNC 50-ohm shielded coax cable. This cable is connected from "CRT" at the rear of the system box to "VIDEO" at the rear of the display unit, for 2511-2010 Backplanes and to the backplane for 2511-2014 Backplanes..

2.8 POSITIONING INTERNAL SWITCHES

2.8.1 CDC Drive

NOTE

The following information is an excerpt from the Control Data Corporation (CDC) documentation package. For further information on the CDC drives, refer to GR stock number #1765-3238.

If a second drive is added, the standard resistor terminator pack (U7) must be removed from drive zero and mounted on drive one (U7).

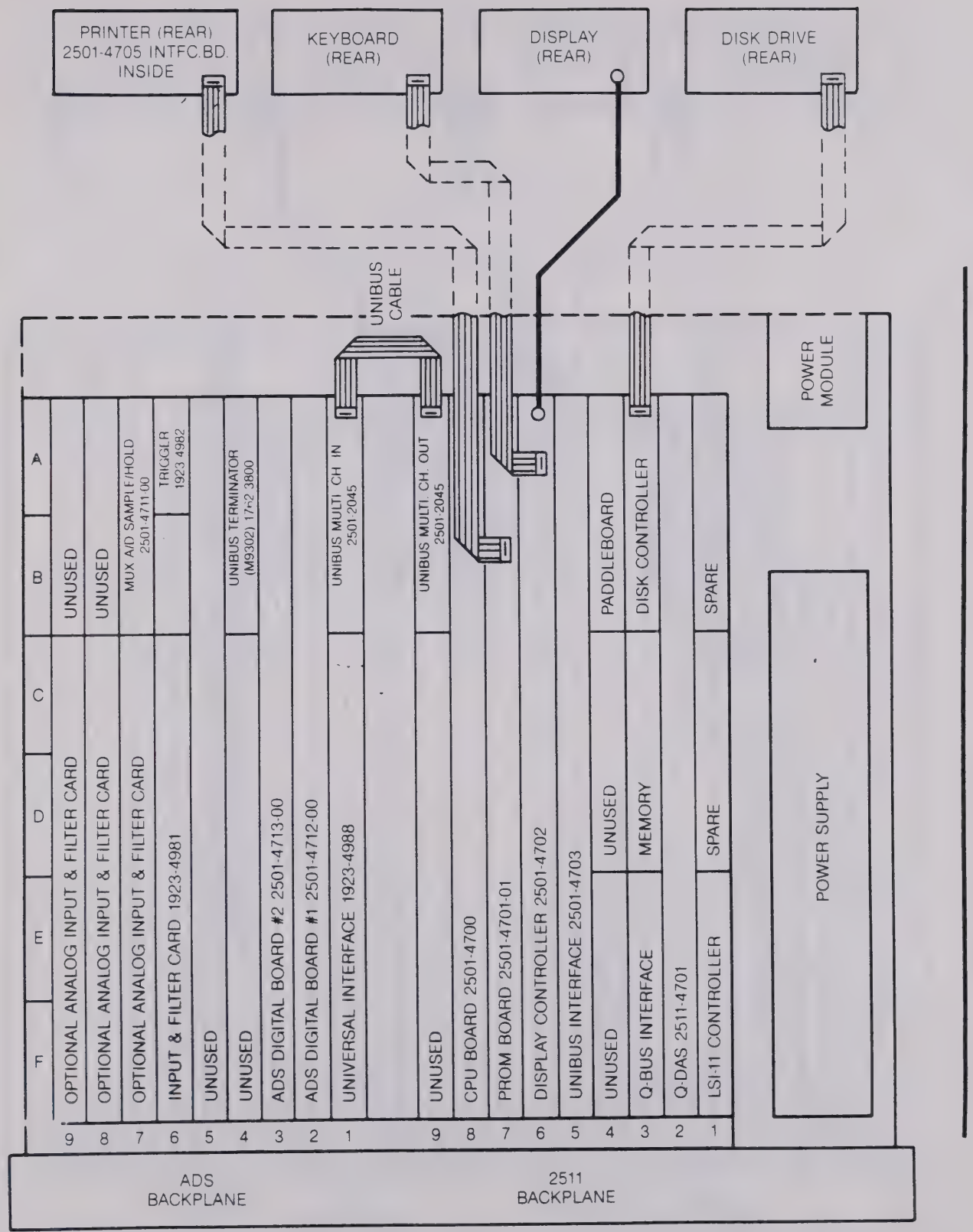


Figure 2-1. Card Locations and Peripheral Interconnect Cabling, Revision 1 Backplane (Long Q-U Cable) 2511-2010/1

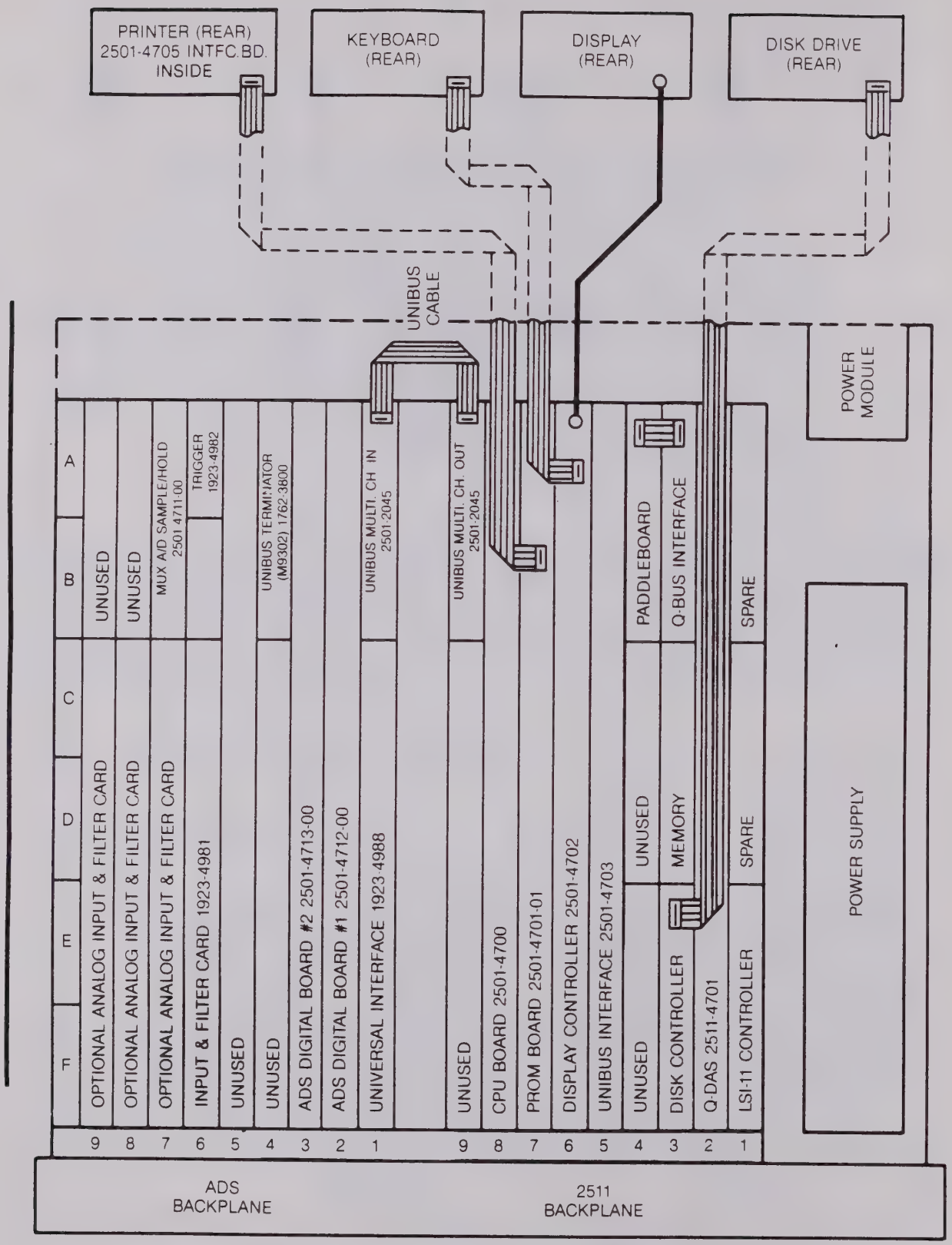


Figure 2-2. Card Locations and Peripheral Interconnect Cabling, Revision 1 Backplane (Short Q-U Cable)
2511-2010/1

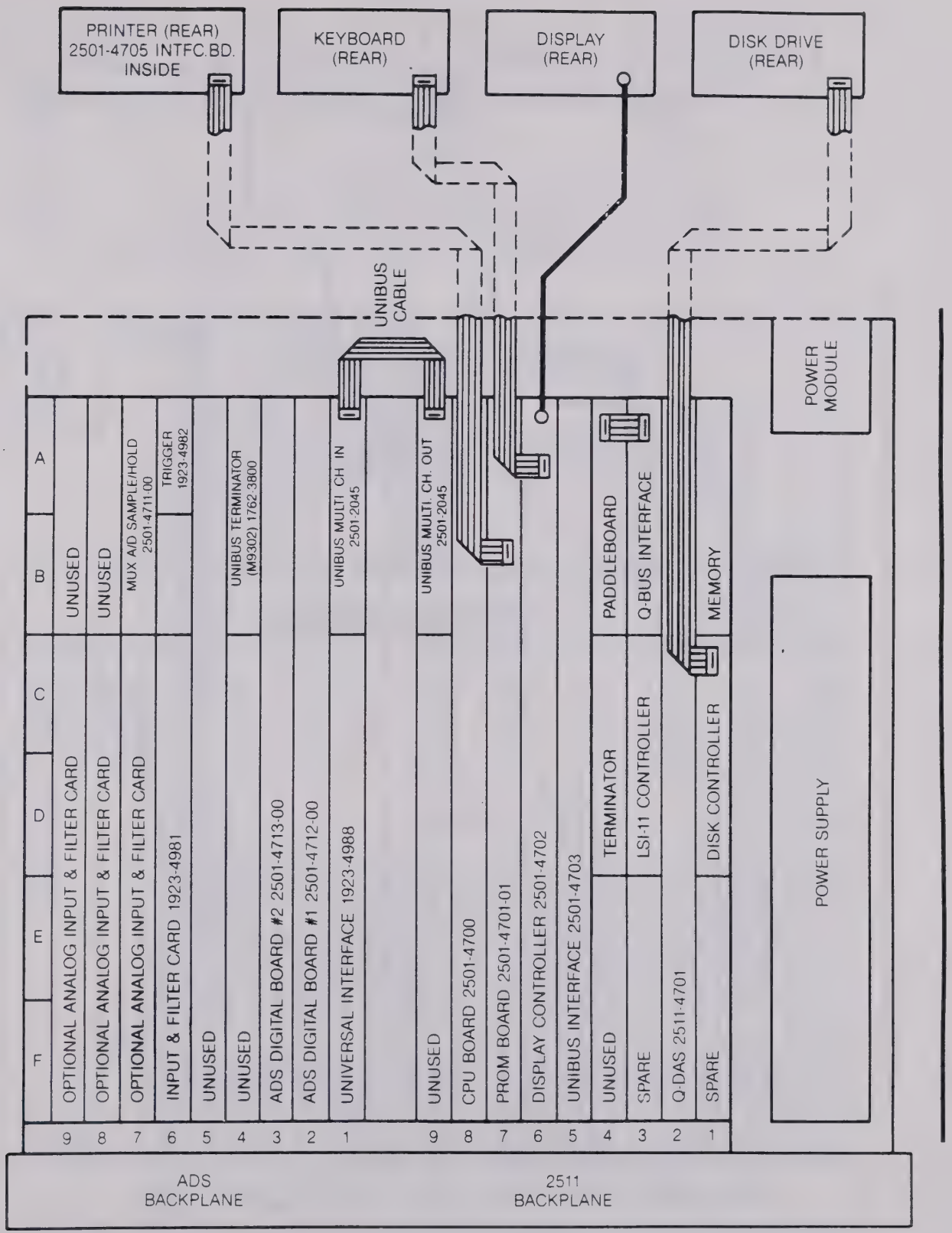


Figure 2-3. Card Locations and Peripheral Interconnect Cabling, Revision 2 Backplane
2511-2010/2

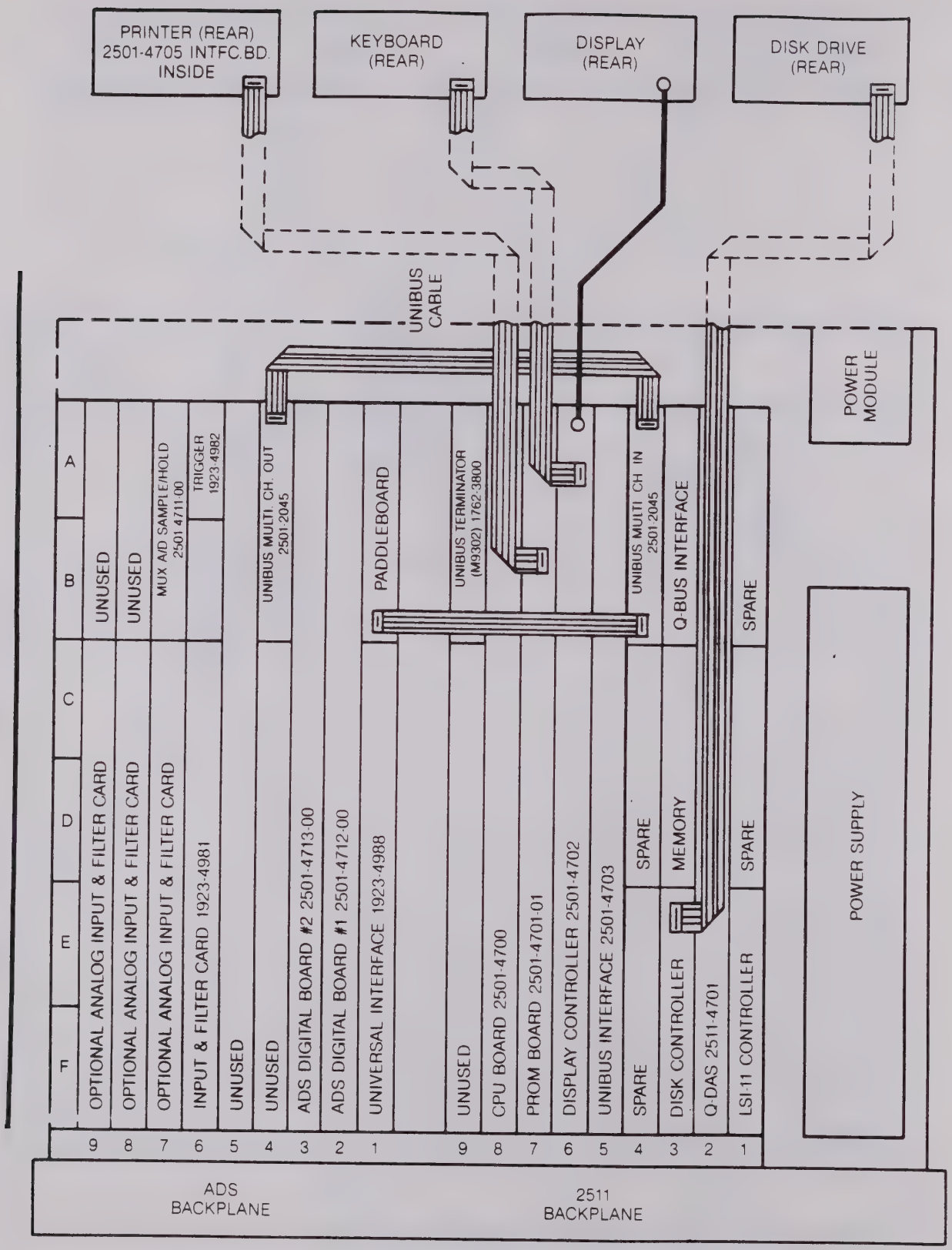


Figure 2-4. Card Locations and Peripheral Interconnect Cabling, 2511-2014 Backplane

2.8.2 Universal Interface Board (2501-4703)

Set switch S1 to the open position.

NOTE

The 2511/2514 VCS may be delivered with any one of several memory board xtpes. Therefore, the DIP switch settings for all are provided below.

2.8.3 DEC Memory Board (32 K) (MSV11-DA, -DB, -DC, -DD or M8044-A, -B, -C, -D Configuration Guide)

NOTE

The following information is an excerpt from the DEC configuration sheet, for further information on the DEC memory board refer to GR stock #1762-4395.

The DIP switch settings for the various memory sizes are listed below:

	Switch Settings					Banks Selected			
Starting Address	S1-1	S1-2	S1-3	S1-4	S1-5	-DA	-DB	-DC	-DD
(32K) 00000	on	on	on	on	on	0	0-1	0-3	0-7
(64K) 20000	on	on	on	on	off	1	1-2	1-4	1-10
(96K) 40000	on	on	on	off	on	2	2-3	2-5	2-11
(128K) 60000	on	on	on	off	off	3	3-4	3-6	3-12

NOTES

- The present range of addressing for the LSI-11 is through bank 7. Bank 7 is normally reserved for peripheral devices. Therefore, the MSV11-D series memories are designed to disable themselves whenever a received address is a bank 7 address (i.e., bus signal BBS7 is asserted). Because of this feature, it is not necessary, nor is it possible, to disable any banks of memory which overlap bank 7 or higher.

- Bus Address Lines (BAD) 16 and 17 are used by the MSV11-D memories. These lines are properly terminated by Revision E KD11-F CPU's and by the KD11-HA CPU. However, Revision C and D KD11-F's do not terminate these lines. If BAD 16 and 17 are not termianted, erratic oepration will occur. With a Revison C and D KD11-F, a terminator module such as the TEV11, REV11-A or the BCV1B cable set must be used.

2.8.4 DEC Memory Board (64K)

NOTE

The following information is an excerpt from the DEC Microcomputers and Memories handbook.

Jumpers and Functions

Function Type Memory	Jumper Configuration	Normal Condition
Non parity	9 to 10	in
With parity	11 to 10	out
Parity nonCSR	18 to 19	in
Parity with CSR	20 to 19	out
Parity Error Report		
Reported BDAL 16L NonCSR	3 to 2	in
Reported BDAL 16 L and BADL 17L with CSR	1 to 2	out
Write Wrong Parity		
Diagnostic bit for tester use:		
Disable	8 to 7	in
Enable	6 to 7	out
CSR Selection		
NonCSR	J to H	in
With CSR	F to H	out
Peripheral Page Selection		
2K peripheral page	29 to 28	out
4K peripheral page	27 to 28	in
Full or One-Half Memory Selection		
Half memory selection (64K)	32 to 33	in
Full memory selection (122K)	34 to 33	out
Removal of Lower or Upper Bank (with a Fault)		
Lower bank has failed	17 to 16	out
Normal operation or upper bank has failed	15 to 16	in
Extended or Normal Memory Selection		
(Small system) normal operation (128K)	R to T	out
(Large system) extended operation (2 meg. words)	R to T	in

2.8.4.1 Partial Starting Address (PSA) Jumpers.

Partial Starting Address (PSA)		Jumpers in (X) to Ground (U)					
Decimal (K)	Octal	DAL Pins	17 Z	16 Y	15 X	14 W	13 V
0	00000000						
4	00020000						X
8	00040000					X	
12	00060000					X	X
16	00100000				X		
20	00120000				X		X
24	00140000				X	X	
28	00160000				X	X	X
32	00200000			X			
36	00220000			X			X
40	00240000			X		X	
44	00260000			X		X	X
48	00300000			X	X		
52	00320000			X	X		X
56	00340000			X	X	X	
60	00360000			X	X	X	X
64	00400000		X				
68	00420000		X				X
72	00440000		X			X	
76	00460000		X			X	X
80	00500000		X		X		
84	00520000		X		X		X
88	00540000		X		X	X	
92	00560000		X		X	X	X
96	00600000		X	X			
100	00620000		X	X			X
104	00640000		X	X		X	
108	00660000		X	X		X	X
112	00700000		X	X	X		
116	00720000		X	X	X		X
120	00740000		X	X	X	X	
124	00760000		X	X	X	X	X

2.8.4.2 Power Jumpers.

Voltage Connection	Jumper Configuration
+5V Nonbattery backup	26 to 25 In (W1)
+5V Battery backup	25 to 25 (W2) 14 to 13 (W3)* or 12 to 13 (W4)*

*Availability for the +5V battery backup

2.8.5 Plessey Memory Board (64K & 128K Word)

The switch/jumper settings that are applicable to the 2511/2514 systems are shown in boldface type.

NOTE

The following information is an excerpt from the Plessy PM-SV128 MOS Memory Manual.

2.8.5.1 Q-Bus (18 bit addressing) Jumper Configuraton.

Jumper	**18 Bit**	22 Bit
W3	**1**	0
W4	**0**	1

Note: 0 = jumper removed
1 = jumper installed

Jumper	**Disabled**	Enabled
W13	**1**	0
W14	**0**	1

Note: 0 = jumper removed
1 = jumper installed

2.8.5.2 Jumper Settings for Battery Backup.

Jumper	Enabled	**Disabled**
W15	1	**0**
W16	0	**1**

Note: 0 = jumper removed
1 = jumper installed

2.8.5.3 Jumper Settings for Parity Versus Non-Parity.

Jumper	Parity	**Non-Parity**
W5	1	**0**
W6	0	**1**
W9	1	**0**
W10	0	**1**
W11	0	**1**
W12	1	**0**

Note: 0 = jumper removed
1 = jumper installed

2.8.5.4 Factory Jumper Configurations.

Jumper	256 P -100	128 P -101	256 N-P -200	**128 N-P -201**
W1	1	1	1	**1**
W2	0	0	0	**0**
W3	1	1	1	**1**
W4	0	0	0	**0**
W5	1	1	0	**0**
W6	0	0	1	**1**
W7	1	1	1	**1**
W8	0	0	0	**0**
W9	1	1	0	**0**
W10	0	0	1	**1**
W11	0	0	1	**1**
W12	1	1	0	**0**
W13	0	0	0	**0**
W14	1	1	1	**1**
W15	0	0	0	**0**
W16	1	1	1	**1**
A	1	1	1	**1**
B	1	1	1	**1**
C	1	1	1	**1**
D	1	1	1	**1**
E	0	0	0	**0**
G	1	1	1	**1**
H	1	1	1	**1**
I	1	1	1	**1**
J	1	1	1	**1**
K	0	0	0	**0**

Note: Jumpers W1 through W16 -
0 = jumper removed
1 = jumper installed

Note: Jumpers A through J -
0 = no jumper to ground installed
1 = jumper to ground installed

Jumpers F and L = ground

Note: Jumpers A through L are either jumpered to ground (pin F or L) or not jumpered to ground. The desired pins to be jumpered to ground should be done so in a "DAISY-CHAIN" fashion.

2.8.5.5 Starting and Ending Address Switch Jumper Settings. The starting and ending address switch/jumper settings for the PM-SV128 memory when installed in an LSI, 18-bit, Q-bus system are as follows:

18-bit Address	Starting Address									
	A	B	C	D	2	3	4	5	E	10
Address Kbytes	Ending Address									
	G	H	I	J	9	6	7	8	K	-
0	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**1**	**0**	**1**
8	0	0	0	0	0	0	0	0	0	0
16	1	0	0	0	0	0	0	0	0	0
24	0	1	0	0	0	0	0	0	0	0
32	1	1	0	0	0	0	0	0	0	0
40	0	0	1	0	0	0	0	0	0	0
48	1	0	1	0	0	0	0	0	0	0
56	0	1	1	0	0	0	0	0	0	0
64	1	1	1	0	0	0	0	0	0	0
72	0	0	0	1	0	0	0	0	0	0
80	1	0	0	1	0	0	0	0	0	0
88	0	1	0	1	0	0	0	0	0	0
96	1	1	0	1	0	0	0	0	0	0
104	0	0	1	1	0	0	0	0	0	0
112	1	0	1	1	0	0	0	0	0	0
120	0	1	1	1	0	0	0	0	0	0
128	**1**	**1**	**1**	**1**	**0**	**0**	**0**	**0**	**0**	**0**
136	0	0	0	0	1	0	0	0	0	0
144	1	0	0	0	1	0	0	0	0	0
152	0	10	0	1	0	0	0	0	0	
160	1	1	0	0	1	0	0	0	0	0
168	0	0	1	0	1	0	0	0	0	0
176	1	0	1	0	1	0	0	0	0	0
184	0	1	1	0	1	0	0	0	0	0
192	1	1	1	0	1	0	0	0	0	0
200	0	0	0	1	1	0	0	0	0	0
208	1	0	0	1	1	0	0	0	0	0
216	0	1	0	1	1	0	0	0	0	0
224	1	1	0	1	1	0	0	0	0	0
232	0	0	1	1	1	0	0	0	0	0
240	1	0	1	1	1	0	0	0	0	0
248	0	1	1	1	1	0	0	0	[illegible]	0
256	1	1	1	1	1	0	0	0	[illegible]	0

Note

Switch = S2

Numbers = switch positions
0 = off
1 = on

Letters = jumpers
0 = jumper to ground removed
1 = jumper to ground installed

Ground = pins F and L

2.8.6 **Dataram Memory Board** (DR-115S)

NOTE

The following information is an excerpt from the DATARAM documentation package. For further information on the DATARAM memory board refer to GR stock #1762-4310.

The DIP switch settings for the various memory sizes are listed below:

	Switch Settings				
Memory Size	1	2	3	4	5
0-32K	off	off	off	off	off
32-64K	off	off	off	on	off
64-96K	off	off	off	off	on
96-128K	off	off	off	on	on

2.8.7 AED Controller

NOTE

The following information is an excerpt from the Advanced Electronic Design, Inc. (AED) documentation package. For further information on AED controller refer to the GR stock #1765-3237.

The following jumper connections must be made on the AED controller.

E2 to E3	Auto Boot.
E4 to E5	Standard Address Vector.
E7 to E8	Enable standard floppy address and vector.
E10 to E11	Disable 22-bit addressing.
E12 to E13 E14 to E15 E16 to E17	AED Manufacutring test only.

2.8.8 Processors

DEC Nomenclature	GenRad Order Part Number
LSI-11/2	2510-2020
LSI-11/23	2511-4711
LSI-11/73	2511-4705

The LSI-11/73 operates only with the 2511-2014 Backplane.

2.9 AC POWER DISTRIBUTION

In a standard configuration, all units are powered through the ac circuits of the Power Module mounted at the rear of the system box. If all unit circuit breakers and power switches are set on, the system is controlled by the single front panel switch and all units power up together. Check the customers electrical service to ensure that the ac power line has proper ac voltage and phasing and is properly grounded.

NOTE

Check that all of the units are set for 115 V or 230 V supply as appropriate, particularly the display unit which has a rear panel slide switch for voltage selection.

Connect the main power cord to ac service and power up the system. Check that all of the units have power and that all fans are operating.

2.10 CALIBRATION

Perform the Calibration procedures as described in Chapter 4 of this manual.

2.11 DIAGNOSTICS

Load and run the diagnostics as described in GenRad's 2511/2514 System Diagnostic Manual, Form #2511-0690. Record all Diagnostics actually run along with any failure information and corrective action taken during diagnostics on the FSR form. Rerun all applicable unit diagnostics before continuing. If a problem is severe (and could result in extended repair or down time), notify the Field Service Branch Supervisor or Branch Manager.

2.12 SYSTEM CHECKOUT

Have the customer help run the receiving checkout tests (RCTs) for all of the software supplied. Ensure that all paper work is complete. (The FSR should reflect any problems/repairs encountered during the installation.) Have the customer sign the FSR and Acceptance form.

2.13 CLEAN UP

Clean up the area around the system. If the area requires more than just picking up, notify the customer so he can schedule the necessary action. Also, ensure that the system is free of finger prints and smudges; touch up where required.

CHAPTER 3 — THEORY

This chapter contains general functional and circuit board descriptions for the GenRad manufactured components; specifically:

Section 1 — Analog-Digital Subsystem (ADS)

Section 2 — Q-Bus Digital-Analog Subsystem (Q-DAS)

Section 3 — GenRad 2501 Microprocessor

Both the Analog-Digital Subsystem and the GenRad 2501 Microprocessor are designed to be interfaced to the rest of the system via the DEC PDP-11 Unibus structure, which in turn is connected to the LSI-11 controller through a "Q-bus" to Unibus converter. The Digital-Analog subsystem is designed to interface directly to LSI-11 Q-bus. The user is presumed to have a working knowledge of the LSI-11, Q-bus, and Unibus operations, and of the various IC chips used in the system. Refer to the 2511-0100 Operating Manual for a simple block diagram description of the complete system, and to vendor manuals for details of the other components. The detailed circuit board schematics and parts lists referred to here are in the separate System Reference Manual.

SECTION 1

ANALOG-TO-DIGITAL SUB-SYSTEM

3.1.1 Introduction

The Analog-to-Digital subsystem (ADS) is designed to acquire and digitize input analog signals from external monitoring devices such as accelerometers, and to pass on this digitized data to memory for subsequent digital processing. The ADS contains all of the necessary control and monitoring logic to accommodate the preselection of various sampling parameters. The ADS contains five major parts, which are controlled through the various application programs. They are:

A programmable amplifier for each input channel, which selects the input range and adjusts the input signal level such that all ranges have the same full scale amplitude at the input to the following A/A filter and analog to digital (A/D) stages. Seven ranges are provided, in binary steps from ±125 mV peak to ±10 V peak, to allow preservation of maximum dynamic range for various signal levels.

A programmable low pass anti-aliasing (A-A) filter for each channel. Aliasing is a phenomenon whereby components in the input signal that have a frequency greater than half the sampling rate will "fold" down into the analysis range and erroneously appear to be components of lower frequency within the range. Low pass filtering of the input removes these components before the signal is sampled. Actually, there are two cascaded 6-pole Chebychev filters on each channel, providing rolloff of 96 dB/octave above the cutoff. The cutoff is programmable at approximately 75 frequencies from the lowest range of 10 Hz to the highest of 25 kHz. Together with appropriate combinations of sampling rate, aliased components are kept at least 70 dB down from full scale.

Sampling and Analog to Digital (A/D) Conversion. After the anti-alias filters, the analog input signals are sampled periodically and converted to digital words for storage in memory and subsequent digital processing. As noted in the paragraph on anti-alias filters, the signal must be sampled at a rate at least twice the highest frequency component of interest. In most GenRad applications software, sampling is programmed at 2.56 times the desired bandwidth for additional protection against aliasing, since the anti-alias filter is not perfect and has a rolloff curve. Thus for the maximum filter cutoff setting of 25 kHz, (i.e., bandwidth) sampling is usually progammed at a 64 kHz rate. The ADS unit has a 2-μs, 12-bit A/D converter and uses simultaneous sampling. All channels are sampled in parallel. The held samples are multiplexed to A/D and converted sequentially. Sampling at 2.56 times the analysis bandwidth, the ADS can maintain a bandwidth of 25 kHz for up to four channels.

Trigger Circuit. For transient signal investigations, the start of data acquisition can be triggered. The trigger source may be selected from any of the first three analog input channels, from an external analog trigger input, or from an external digital trigger signal represented by a TTL logic level or switch closure input. For the analog sources, positive or negative slopes, or both, may be selected. The level is programmable at 64 steps between the negative and positive full scale levels. These steps are determined by the input amplifier setting, except for the external analog trigger input. This input has a fixed range of ±2 V. In conjunction with the control logic, a transient capture mode may be selected. In this mode, the start of the acquisition input record blocks can be advanced or delayed in time from detection of the specified triggering conditions.

Control and Interface Logic. This final section contains the control registers for programming the conditions in the previously described sections, and the direct memory access interface logic for transferring input samples to memory over the Unibus. Included are the word count logic for specified input record sizes, the addressing and sorting logic for generating memory putaway addresses and separating multi-channel input records, and the buffer swapping logic for the double buffer input mode that allows continuous data acquisition while processing is in progress. The control logic section also provides error detection logic for conditions such as illegal range, filter, or sampling rate setups, overranging of the input signal (saturated full-scale A/D output), or loss of an input sample due to bus access problems. Input frame sizes are selectable from 128 to 16K points in binary steps. Sample periods range from $\simeq$16 μs to $\simeq$ 100 ms. The FIFO buffer assures compatibility with most bus configurations (up to $\simeq$16 μs latency acceptable).

NOTE

The backplane and circuit boards of the 2511/2514 ADS are the same ones used in the "multichannel" ADS of larger 2500-series systems. The ADS control and sampling circuitry is capable of handling up to 8 channels by the addition of another backplane and 4 more input boards in the larger box systems. References to more than 4 channels are not applicable for 2511/2514 systems.

3.1.2 ADS Control Register Bus Addresses and Bit Assignments

Figure 3-1 shows the ADS control register functions and addresses. The following paragraphs describe the registers and bits individually as introduction to the functional descriptions that follow.

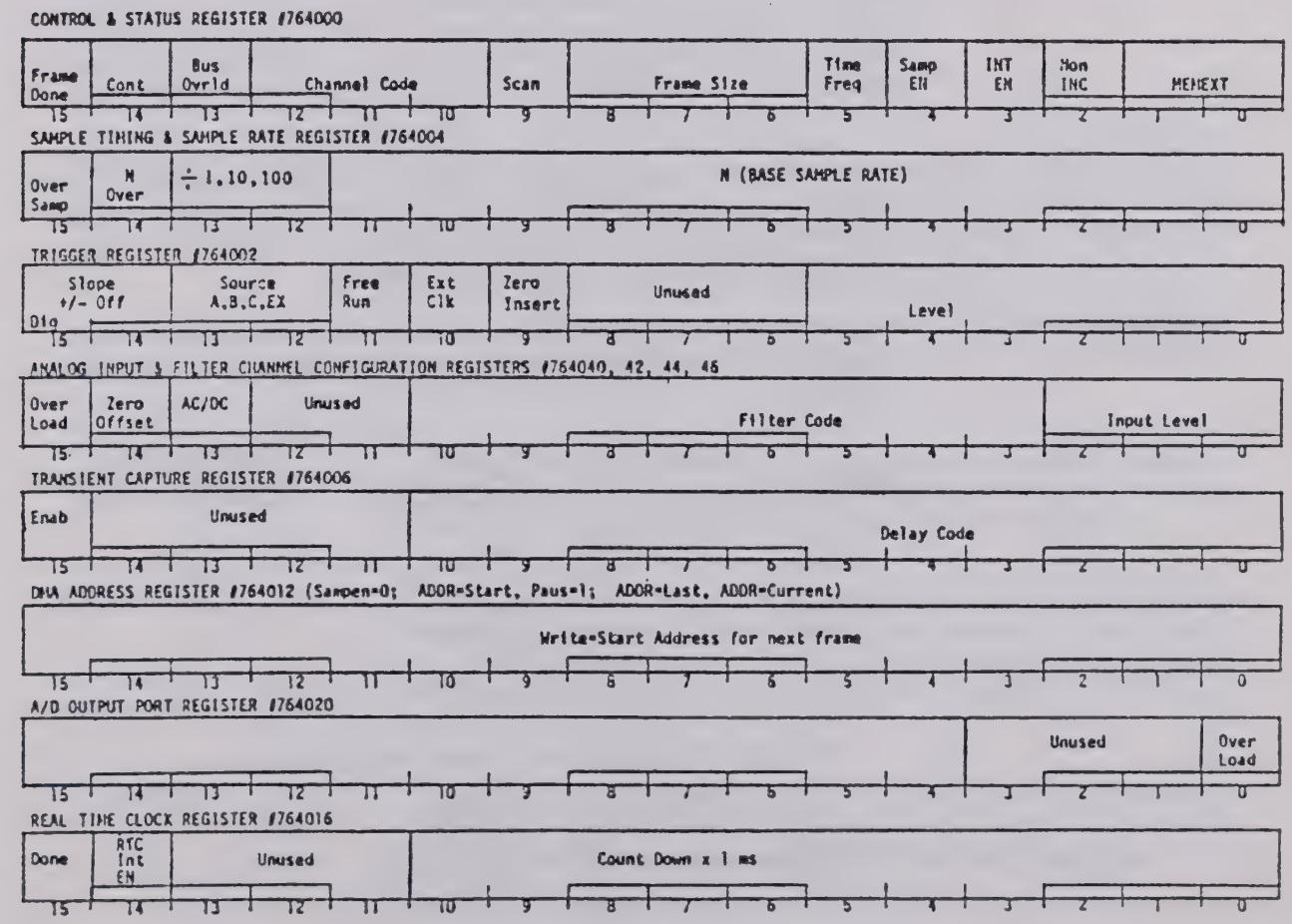
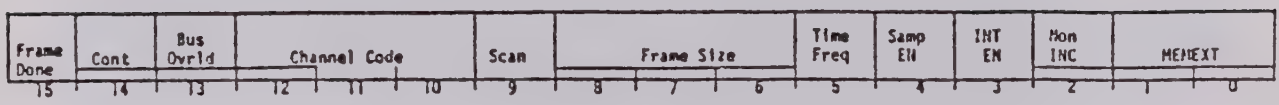


Figure 3-1. ADS Control Registers

3.1.2.1 Control & Status Assignments Register (764000)



DONE/CONT

The frame done bit is set on completion of an input data frame. If CONT (continue) is not set, data acquisition stops when Done is set. If Cont is set, data acquisition will continue. If at the end of the "continued" data frame, Done is still set, Cont will be cleared and data acquisition will stop. Done must be cleared under program control. Cont is cleared by clearing Done. Discontinuous operation can be determined by checking Done at the end of the process interval. If Done is already set data has been lost; consequently the Cont bit need not be set, though it may be if care is taken to set it prior to clearing Done. If set after or at the same time, Cont will cause data acquisition to continue into the area currently being processed.

BUS OVLD

When the BUS OVLD bit is set, it indicates that the FIFO storage buffer was full when a new input was requested. In terms of the Unibus, it indicates that the ADS system waited longer than 16 μs to become bus master. In effect, the bus cannot handle the data at the rate requested.

CHANNEL CODE
SCAN

The Channel Code word represents the number of channels to sample if Scan is set; it represents the channel to be sampled if Scan not set.

Channel Code	Scan = 1 No. of Channels		Scan = 0 Channel Sampled
000	00	(A)	A
001	02	(AB)	B
010	04	(ABC)	C
011	06	(ABCD)	D

NOTE

The 2511/2514 systems utilizes only channels 1-4.

100	10	(ABCDE)	E
101	12	(ABCDEF)	F
110	14	(ABCDEFG)	G
111	16	(ABCDEFGH)	H

FRAME SIZE

The frame size is determined by bits 06, 07 and 08 as follows:

08, 07, 06	Words
0 0 0	128
0 0 1	256
0 1 0	512
0 1 1	1024
1 0 0	2048
1 0 1	4096
1 1 0	8192
1 1 1	16384

FREQ

When set, all time base values are derived from 4.096 MHz clock. When cleared they are derived from 4.0 MHz clock, except real time clock which always references 4.096 MHz to derive 1 ms as:

$$\frac{4.096\text{MHz}}{4096} = 1\text{kHz}$$

SAMP EN

This is the primary enable for the system. When cleared, all address counters are reset to their base addresses. Buffer counters are loaded to frame size values, and all data transfers are inhibited, as is the DONE interrupt. In the event that single buffer operation is desired, SAMP EN may be cleared between sample intervals to reset address counters. When set, sampling and DMA operations are enabled. Subject to other conditions, sampling may begin.

DONE INT EN

When set, this bit enables an interrupt upon the completion of a frame. If set following a frame end, it will not "remember" even though DONE bit has not been cleared.

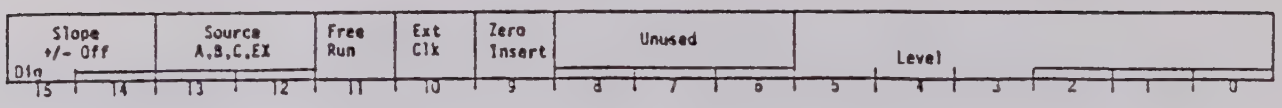
NON INC

This bit inhibits the memory address count. All data will be loaded into the base address. It may be changed in the midst of data acquisition, though if multiple channels are being input, they may be scrambled — certainly less than a full frame will be acquired.

MEMEXT

Memory management bits for extended memory. These are affected by address counter; hence, data buffers which cross memory management boundaries (32K) are not allowable.

3.1.2.2 Trigger Mode Register (764002)



SLOPE — Selects trigger slope:

00 - digital trigger input
01 - negative slope
10 - positive slope
11 - positive or negative slope

SOURCE — Selects trigger source:

00 - 1
01 - 2
10 - 3
11 - EXT

FREE RUN — When set, sampling will start as soon as SAMP EN is set. If cleared, sampling starts upon receipt of a trigger input. If not set after sampling begins, each new frame must be triggered (Trig every frame). FREE RUN also unconditionally enables the sample generator, hence other circuits using the +SAMP signal may function even if sampling is not enabled.

EXT CLK — When set this bit allows the input of an external pulse to generate the sample command. (The actual sample will be taken 2 µs ±.250 µs following the high to low transition of the input signal.) This enable also changes the 'N' readback in the Sample Rate word to a frequency counter to determine the period of the incoming Samp pulses.

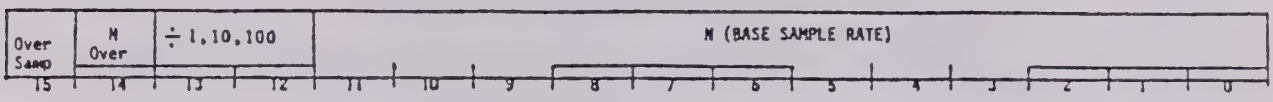
ZERO NST — Enables zero "insertion". Frame sizes double - intervening locations are skipped, not zeroed, so the program must zero memory before starting.

TRIGGER LEVEL — Selects trigger level +Full scale to -Full scale in 64 steps of 1.56% each:

000000 - + FULL SCALE
000001 - 90.44%
100000 - ZERO
100001 - -1.56%
111111 - - FULL SCALE

(Absolute Accuracy ±5%)

3.1.2.3 Sample Timing and Sample Rate Register (764004)



OVERSAMP — When set, this bit indicates the sampling rate is too high

$$fs = \frac{10^6}{(4.1 + 2.9\ N)} \text{ maximum}$$

where N = number of channels. This flag valid at all times, including EXT samp. Must be cleared by resetting SAMP EN, i.e., bit 04 register -00.

N OVER — Valid only for EXT SAMP, this bit indicates that the frequency counter (N) has overflowed. This bit is cleared by writing into the Sample Rate register (used only with external sample).

SAMP MULT — Selects the factor to multiply the base sample rate (4.0 MHz or 4.096 MHz as selected by FREQ bit of Control and Status register):

Sample Multiplier		Factor	U45-15 Carry Out 4.0 MHz	U45-15 Carry Out 4.096	Counts	Configuration U45	Configuration U44
13	12					128 - 16	8 - - 1
0	0	X1.0	.250 µs	.244 µs	(1)	1 1 1 1	1 1
0	1	X0.1	2.250 µs	2.440 µs	(10)	1 1 1 1	0 1 1 0
1	0	X.01	38.5 µs	37.576 µs	(154)	0 1 1 0	0 1 1 0

N (Base Sample Rate) Selects the sample frequency by the following formula:

$$f_S = \frac{\text{(SAMP MULT) X (4.0 or 4.096 MHz)}}{(4097 - N)}$$

Note that the maximum legal sample rate is $\frac{10^6}{(4.1+2.9*N)}$

where N = number of channels

3.1.2.4 Analog Input and Filter Registers (764040-56)

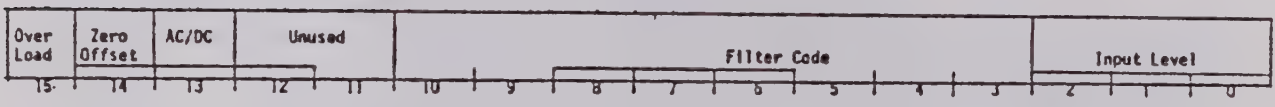
CHANNEL CONFIGURATIONS

MASTER	CH	(SLAVE	Not applicable to the 2511/2514 System)
764040	1	764240	
42	2	42	
44	3	44	
46	4	46	

NOTE

The 2511/2514 system utilizes only channels 1-4.

50	5	50	
52	6	52	
54	7	54	
56	8	56	



OVERLOAD — Indicates that an input on some channel overloaded Full Scale ± 4LSB during the last input frame (not the one in progress). Updates automatically (on a sample/channel basis, the overload is indicated by the LSB of the data word).

ZERO OFFSET — A common bit between all channels, this bit should always be set when changing configuration. Further, whenever processing time permits, it should be set to minimize offset drift. When set on any channel, a hardware algorithm is initiated to zero dc offsets. The inputs are isolated and shorted, and sampling is started. When all selected channels read zero, the zero offset bit clears. This is the "ready" signal indicating that dc offsets are zeroed and that processing may proceed.

NOTE

The hardware assumes that the filters and sample rates correspond for minimum time to perform the zeroing operation. If time is critical, set the sample rate to the maximum legal rate, and set the filter to all-pass.

Zeroing will take place on the channel or channels previously selected (be sure you want to do that). If for any reason the circuitry cannot zero (hardware failure), the offset zero operation can be terminated by writing a zero into the offset bit (time out loop is a good idea for this). If this is done, the particular channel in error can be isolated by selecting single channels to try to zero.

AC/DC — When set, selects dc coupling, when cleared selects ac.

FILTER CUTOFF CODE — An eight-bit code to select filter cutoffs. The first three bits select the capacitor, the last five the resistor combinations. Following are some representative combinations:

100	00001	.01 kHz
010	00001	.1 kHz
001	00001	1 kHz
001	00010	2 kHz
001	00100	4 kHz
001	01000	8 kHz
001	10000	10 kHz
001	11111	25 kHz
000	xxxxx	All Pass
xxx	00000	None Pass, Produces Overload

NOTE

Bit 6 is only weighted as 10 instead of 16 as binary indicates. Note also that only one capacitor (bits 9,8,7) is selected at a time, and that an all 0 resistor code (bits 6-2) disconnects the signal from the filter output.

INPUT LEVEL — Sets the Full Scale of the preamplifier.

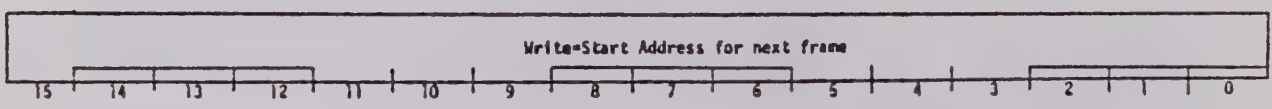
000	=	±16V
001	=	± 8V
010	=	± 4V
011	=	2V
100	=	1V
101	=	0.5V
110	=	0.25V
111	=	0.125V

3.1.2.5 Transient Capture Register (764006)

ENAB — The basic operation is to take X samples following a trigger (transient) input. Until the transient occurs, data is taken in a circular buffer. A trigger occurring before one buffer of data is taken will be ignored. After at least one buffer, the trigger will then be followed by X additional samples; transient enable will be cleared, and Done will be indicated. (At this point the DMA start address may be interrogated to determine the start of the data in the circular buffer.)

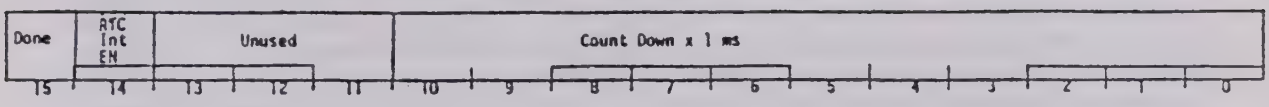
DELAY CODE — The eleven bit DELAY CODE determines the number of samples that will be taken following the transient. Note that the delay code is destroyed following the operation, so that successive operations must re-load the DELAY CODE.

3.1.2.6 DMA Address Register (764012)



For writing, the word indicates the base address of the data block. It need not be loaded for each frame, and may be loaded while sampling in progress (in this case the next frame will use the loaded base address - be careful if double buffering). When reading, the data is the start address if not sampling, or if in PAUS mode and not transient capture. Note that the address read is always the base counter address - offsets for multiple channels, double buffering or zero insertion cannot be read. For Transient Capture, the buffer start address must be read before clearing Done.

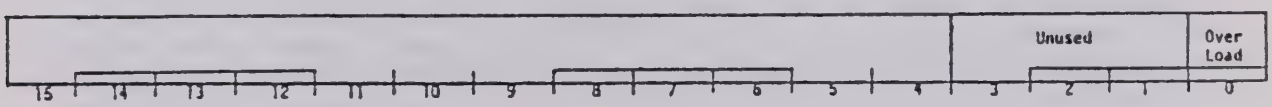
3.1.2.7 Real Time Clock Register (764016)



Provides continuous count down of 1 ms pulses derived from basic system clock.

DONE	Set when down counter reaches zero. Counter continues.
RTC INTEN	Enables interrupt when counter reaches zero.
COUNT DOWN X1ms	12 bits may be loaded and counted down - not adequate for long term time-keeping (possible error of 10 seconds/day)

3.1.2.8 A/D Output Test Port Register (764020)



This register is used only for diagnostic purposes. It allows the user to read each sixteenth word output from the A/D to the FIFO while under program control.

OVERLOAD	The OVERLOAD bit is set when the A/D circuit is saturated.

3.1.3 Overall Functional Description

For a detailed block diagram and circuit board schematics of ADS, refer to the following drawings in the Diagrams and Parts Lists volume:

ADS Detailed Block Diagram	2501-3029-6D
Analog Input and Filter Board	1923-4981-2D
Sample/Hold and A/D Board	2501-4711-2D
Trigger Board	1923-4982-2D
Control Board #1	2501-4712-2D
Control Board #2	2501-4713-2D
Universal Interface Board	1923-4988-2D

Initiation of sampling can occur either as a "freerunning" or "triggered" event. When "triggering" is selected, it may be based on a particular channel source (764002, bits 12 and 13), its polarity/slope (76400, bits 14 and 15) and its relative input level (764002, bits 0 through 5). The analog input signal from the A/A filter is routed to the trigger circuit (1923-4982) for this purpose. The term "TRIG" is generated on the preceding conditions and is routed to the Sample Control Logic (2501-4713). The Sample Control will enable the Sample Timing and Sample Generator circuits as soon as it receives "TRIG" as long as it is "Sample Enable", until a "Full Buffer" indication is received. The Sample Timing logic issues a "+SAMP" pulse at intervals from 16 μs to 100 ms depending on the sample rate selected (764004). Because the minimum period required for conversion of the analog sample to its digital equivalent is approximately 8 μs, it is invalid to select any sample rate faster than 8 μs.

The conditioned analog outputs from the anti-aliasing filters are fed to the sample and hold (S/H) circuitry. The Sample Generator then issues the "HOLD" control signal to the S/H circuitry at intervals designated by the Sample Rate Register (764004). Immediately following the "HOLD" command, the Sample Generator issues a Start Convert Pulse (+STCVTP) and the amplitude of the input analog signal held in the S/H is fed to the A/D circuitry where it is converted to a digital value in terms of 12 binary positions. The channel selector register (764000) can be programmed to continually feed a single channel or up to 8 analog inputs into the A/D. If multiple channels are being scanned (+SCAN active), the Sample Generator will multiplex the analog amplitudes held in the S/H to the A/D. An "OVERSAMPLE" condition will occur if a (+SAMP" signal is issued to the Sample Generator before it has completed a previous Hold/Convert sequence. The digital output value of the A/D is fed to a sixteen word "First-In First-Out" (FIFO) buffer along with the End of Convert (EOC) control signal. The data is stored in the FIFO while a DMA is requested to move it into memory.

A unique interaction of the Trigger and Channel Scan Logic is introduced into the DMA address control circuit. This interaction provides for a channel addressing offset scheme to insure discrete memory addressing for each active channel. Upon completion of each frame of data (-FULLBUF), a "STOP" command is issued by hardware which causes the Sample Control logic to revoke the "+TRIGGERED" signal, shutting down the Sample Generator and setting the "DONE" status flag (764000, bit 15).

If sampling is required on a continuous (Real Time) basis, a "CONT" flag (764000, bit 14)may be set under program control which will permit data sampling to continue with the acquisition of the next frame of data. If however, the operating software does not service (reset) the "DONE" flag before the "Continued" frame of data is complete, the "CONT" flag will reset, halting any further data acquisition. This situation would typically indicate that processing time of a frame of data exceeded acquisition time of a subsequent frame.

3.1.4 **Universal Interface Board** (Schematic 1923-4988-2D)

The Universal Interface (UI) provides the required Unibus protocol for transfer of data IN or OUT of the ADS. All Unibus address and data lines are buffered, and initial device selection is determined in the Universal Interface. Only the lower five address bits (+AI01/+AI05) are passed on to the ADS for decode of specific program registers. All jumpers are defined in 1923-4988-2D. Specific ADS requirements are as follows:

- Unibus address 764000 = Jumper A6, A7, A8, A9, AI0, A12 (for zero's)

NOTE

The omission of the lower five address positions provides a total of 32 register addresses of which 13 are used.

- Read/Write = E31 to E33 and E29 to E30 (word operation only)
- Vector Address 270/274 = V2, V6, V8
- Bus Priority 4 = E15 to E16, E10 to E1, E9 to E5
- DMA Operational = E13 to E14, E20 to E21, E22 to E23, E11 to E12

The Program Register Selection is decoded from a series of binary to decimal elements. Enabling of the array of 7442's is achieved by -REDHI or -WRTLO generated by the Universal Interface to reflect a "DATA IN" or "DATA OUT" condition (+OCO/+OC1). Only when input "D" of U46 is low can any other input be considered. The effect of -WRTLO on input "C" is to select either the low order decode of address bits +AI04/+AI05 (output 0, 1, 2) or its high order equivalent (output 4, 5, 6). In any event, the activity in U46 will enable one (and only one) of the subsequent address selector elements U59/U64 (sheet 1 of 2501-4712).

3.1.5 **Analog Input and Filter Board** (Schematic 1923-4981-2D)

The analog input to the ADS is through the front or back of the system box via four BNC receptacles marked 1 to 4 for each of the respective channels. The signal first appears in the logic as "+ANALOG CHX" and "-ANALOG CHX". Although designed for differential input to reduce noise pick-up, single sided connection can be accommodated by simply grounding the negative line (-ANALOG CHX). The analog input circuitry, including preamp, auto-zeroing circuity and anti-aliasing filter occupies a single four-wide board. The primary input to the circuitry is "Quasi Differential" in that a true differential input circuit exists but the low side (outer shell of the panel BNC) is returned to analog ground through a 10 ohm resistor. A description of each circuit follows.

3.1.5.1 Channel Amplifier. The Channel Amplifier is controlled by 4-bits of the appropriate channel control word - 764040 Channel 1, 764042 Channel 2, etc., and are held static by the corresponding "-WRT X" Command. Bits 0, 1 and 2 determine input sensitivity while bit 13 selects the coupling mode (ac or dc). The input signal is either dc coupled through K2 (76404x, bit 13) or ac coupled via C1 and C2 through K3 (which opens for offset calibration only) and then into the differential amplifier at U2.

The AD521 element at U2 contains the only adjustments in the analog input:

- R5 is a coarse offset adjust.
- R8 is the low range gain adjust.
- R2 is the high range gain adjust.

The adjustment procedures are defined in Chapter 4 - Service.

Relay K1 (76404x, bit 2) defines the gain (input level) for U2. With K1 closed (bypassing R1-R2) a gain of 5 will be achieved, while opening K1 will result in a gain of 5/16. K1 therefore will produce a relative output gain of 16, and should not be invoked with input levels greater than 1 volt. The output of U2 (TP1) is fed into a four channel programmable amplifier (U3) via a precision resistor network (R9). The selection of the active amplifier is determined by inputs "+CHX G0" and "+CHX G1" (76404x, bits 1 and 2). The selection by software of one of these amplifiers will produce a gain (input level) of 8, 4, 2 or 1 (Amp #1) at the output (TP2), relative to the input (TP1). Input Level Selection defines the interaction of both gain control decodes to achieve a full scale output (±5V) from U3, for a specific maximum input level from the external device.

3.1.5.2 Auto Zeroing. A 6-bit D/A converter is used to zero dc offsets (aside from the adjustments provided) that occur in the system. To utilize this feature the control hardware provides signals to isolate the input amplifier from external signals and then checks for the most significant 10 bits of the A/D output to be zero for each channel in use. If not, an up-down counter is incremented to zero the offset.

3.1.5.3 Anti-Aliasing Filters. The anti-aliasing filters are dual six pole Chebyshev filters which are controlled by the Channel Configuration word 76404X, bits 3-10. The control word is held static to provide two groups of filter parameters "+CEN X" (Capacitance) and "+RENX" (Resistance) that activate a matrix of relays. The filter relay configuration shown below shows the bit configuration of the control word vs. the relay activation and frequency cutoff for ten of the 75 possible codes. There is a gain of "1" through the filter, thus the output amplitude should equal input amplitude. The automatic offset input "D/A OUT" is fed into the conditioned analog input "BUF ANALOG CHX" at U1. The amplitude of this signal can add as much as 640 mV to the analog input at this point.

Control Word Bit Positions	CAPACITANCE 10	9	8	RESISTANCE 7	6	5	4	3	Frequency Cutoff f_c
	1	0	0	0	0	0	0	1	.01 kHz
	0	1	0	0	0	0	0	1	.1 kHz
	0	0	1	0	0	0	0	1	1 kHz
	0	0	1	0	0	0	1	0	2 kHz
	0	0	1	0	0	1	0	0	4 kHz
	0	0	1	0	1	0	0	0	8 kHz
	0	0	1	1	0	0	0	0	10 kHz
	0	0	1	1	1	1	1	1	25 kHz
	0	0	0	1	1	1	1	1	All Pass
	X	X	X	0	0	0	0	0	None Pass
	CEN (2)	CEN (1)	CEN (0)	REN (4)	REN (3)	REN (2)	REN (1)	REN (0)	

CEN0 = x 1000
CEN1 = x 100
CEN2 = x 10

REN0 = 1
REN1 = 2
REN2 = 4
REN3 = 8
REN4 = 10

3.1.6 Sample and Hold, Multiplex and A/D Board
(Schematic 2501-4711-2D)

A single two-wide board holds the circuitry necessary to sample and convert from 1 to 8 inputs from the analog input boards. Eight monolithic sample/hold IC's are utilized to simultaneously sample the input signals. The outputs of these are fed into a D-MOS FET multiplexer (U10,11) which sequentially scans the active channels. The output of the multiplexer drives the 12-bit 2 μs A/D converter which sequentially converts the active channels. Approximately 1 μs is allowed for the output of the multiplexer to settle before the conversion is initiated.

3.1.6.1 Input Select. The analog data from the filter, identified as "CHA" through "CHC" is routed to the Trigger Source and the Input Select. Because the ADS can operate in either a single channel or multiple channel scan mode, the Input Select Logic U9 - 12 are high speed FET switches. The output of the FET switches is determined by enable signals EN1 - EN8. These eight enables, one each switch, are derived from the Channel Selector Binary-to-Decimal Decode U64 and U65 from Digital Control Board No. 2 (2501-4713).

Note that the Channel Selector has the capability to select up to 8 channels - "CHAEN through CHHEN". The 2511/2514 systems utilize only four channels (CH 1-4). The Channel Scan Counter U48 (4713) which feeds the Channel Selector, is loaded from the channel code segment of the ADS control and Sample Mode Register 764000 (bits 10, 11 and 12).

3.1.6.2 Analog to Digital Conversion. The A/D element U15 receives the measured analog amplitude from the S&H and performs a 12-bit conversion to binary format. The Start Convert Pulse "+STCVTP" is issued by the Sample Generator approximately .250 μs after "-HOLD". The End-of-Convert "+EOC" signal will be issued by the A/D along with a valid 12-bit binary conversion, less than 4 μs after "+STCVTP". Components U1-8 are eight individual S/H for channels 1-8. Although there are no offset adjustments on the S/H, offset can be measured for each individual sample and hold by connecting a voltage source to TP1-8 and measuring at TP11-18 respectively. Maximum offsets shall not exceed 20 mV. Filter boards should be pulled for the channel under examination. Data is collected simultaneously in the S/H by +HOLD at TP9. The FET switches U9-12 then switch the data to the A/D determined by the channel enables CHXEN at TP21-28. The term MPX OUT delivers the data to the A/D for conversion.

3.1.7 ADS Digital Control Board No.1 (Schematic 2501-4712-2D)

The ADS Digital Board No. 1 consists of the following circuitry: Sample Timing, Frame Size and DMA Address Generation. A description of each circuit is provided below.

3.1.7.1 Sample Timing. The timing generation of the sample pulses (+SAMP) originates from a series of sequential binary counters. The +4MHz clock is the basic ADS timing source. The actual clock interval can be selected for compatibility with either "Time Domain" (250 ns, 4 MHz) or "Frequency Domain" (244 ns, 4.096 MHz) sampling. This is accomplished using +FREQ (764000, bit 5). The +4MHz signal drives an 8-stage binary counter (U44,U45) that is preloaded (764004, bit 12,13) by the sample multipliers to reflect one of the three following base rates:

Sample Multiplier		Factor	U45-15 Carry Out		Counts	Configuration	
			4.0 MHz	4.096		U45	U44
13	12					128 —16	8— 1
0	0	X1.0	.250μs	.244μs	1	1 1 1 1	1 1 1 1
0	1	X0.1	2.250μs	2.440μs	10	1 1 1 1	0 1 1 0
1	0	X.01	38.5μs	37.576μs	154	0 1 1 0	0 1 1 0

The Sample Rate Counter (U50,52,56) is preloaded by the Sample Rate Register (764004, bits 0-11). Since the counter is incremented with each carry out of the Base Rate Counter the desired sample rate is established by dividing the base rate into the desired sample rate to produce the complement of the sample rate register.

The initiation of Sample Timing occurs with the receipt of +TRIGGERED which sets the Start Sample FF (U29 pin 5). This action removes the pre-set input to the TR FF (U29 pin 9), which has been holding both the Base Rate Counter and the Sample Rate Counter in a "Load" state. The next +4MB to arrive after U29 pin 5 sets will reset TR and permit the Base Rate Counter (U44,45) to begin incrementing. Additionally, TR produces the first +SAMP which is routed to the Sample Generator to cause acquisition of the first word of data. Each time the Base Rate Counter advances the Sample Rate Counter to a full count, the carry out of U56 pin 15 will cause TR (U29 pin 9) to set, re-initializing the sample rate counter and Base Rate Counters. On the next +4MB, TR will reset (as long as +TRIGGERED is still available) and the count will begin again as the +SAMP pulse is sent to the Sample Generator to permit acquisition of the next word. The External Sample Counter (U51,55) is used to examine the sampling rate of an external sampling clock and permit programmed inquiry (764004, bits 1-11) of the observed rate. Reference External Trigger segment for details.

3.1.7.2 Frame Size Control. The Frame Size as determined by the program (764000, bit 6, 7, 8) is held static in U35. Because the Frame Size Code, +FRMSZ(0), +FRMSZ(1), +FRMSZ(2) is a binary multiple from 128 to 16,384 words, a BCD to decimal decode IC (U7) will produce a single output corresponding to the frame size selected.

FRAME SIZE DECODE

U7 INPUT			U7 OUTPUT	FRAME SIZE
FRM SZ (2)	FRM SZ (1)	FRM SZ (1)		
0	0	0	PIN 1 LOW	128 WORDS
0	0	1	PIN 2 LOW	256 WORDS
0	1	0	PIN 3 LOW	512 WORDS
0	1	1	PIN 4 LOW	1024 WORDS
1	0	0	PIN 5 LOW	2048 WORDS
1	0	0	PIN 6 LOW	4096 WORDS
1	1	1	PIN 7 LOW	8192 WORDS
1	1	1	PIN 8 LOW	16384 WORDS

The output from the Frame Size Decode logic is always present on the input of the Frame Size counter U5, 6, 15 and 21. Since the output of the Frame Size Decode is "Negative True" logic, the effective configuration presented to the Frame Size Counter will be the "1's" complement of the desired frame size. At the start of each frame (-FRMST) the frame size counter will be loaded with the "1's" complement of the Frame Size. This action occurs initially from +TRIGATE and on subsequent CONTINUOUS frames from U18 being reset with the "Carry Out" of the Frame Size Counter. The Frame Size Counter is incremented by +ADDRCK (U31 Pin 5) under the following circumstances:

- If single channel non-scan operation is selected, the channel code down counter (U47) is set to zero. Each -"DMACK" (DMA CLOCK) will cause a borrow and toggle "+ADDRCK".

- During multi-channel scan operations, the channel code down counter is initially loaded with the number of channels to be scanned. Each DMA generated to support the Scan will decrement the counter until all channels have been sampled and the DMA operation has moved the data to memory. The DMA for the last channel in the Scan will cause the borrow from U47, Toggle "+ADDRCK", and increment the Frame Size Counter.

One important aspect of the control FF "+ADDRCK" should be noted. Since the Frame Size Counter was initially loaded to the "1's" complement, "+ADDRCK" is activated in a Dummy Cycle at the very beginning of the frame by U31 Pin 9 and "-FRMST" to bump the Frame Size Counter by one to achieve a "2's" complement of the Frame Size. This will cause the Frame Size counter to increment the exact number of times to equal the specified frame size before the Carry from U21 terminates the frame.

3.1.7.3 DMA Address Generation. The base address for DMA operations is loaded into the "Base Address Register" U23, 33, and 42 under the control of the operating program (764012). The address generation logic has five modes of operation to accommodate various data acquisition schemes:

(1) **Non-Increment.** In this mode (764000, bit2) the Base DMA Address is transferred into the Address Counter at the start of each frame, but is inhibited from incrementing by U11-5. Thus all data sampled is routed to a single location in memory, regardless of channel selection or frame size.

(2) **Basic Mode.** In its simplest form of operation, the DMA generation logic loads the content of the Base Address Register at the start of each frame (-FRMST) into the Address Counter (U49, 54, 58, 26). During the DMA operations which follow, the content of the Address Counter is "Added" to the output of the offset PROMs. Under the PROMS conditions previously specified, the output of the offset PROMS will always be zero. Thus the content of the Address Counter is unmodified and represents the actual address in the Host Memory. On completion of each DMA, "+ADDRCK" increments, the address Counter to select the next sequential memory address.

(3) **Zero Insert.** When operational requirements dictate the use of the Zero Insert Mode (764002, Bit 9), the amount of memory required for a specified frame size is doubled (i.e., if a 512 word frame size is specified in register 764000, 1024 words of memory are required for each channel being sampled). The term Zero Insert is somewhat misleading since this mode of operation does not actually insert zeros at all. It simply overlays the frames of sampled data on an area of memory which must be previously zeroed by software.

(4) **Scan Mode.** During a Scan mode of multiple channels, the frame size +FRMS=(X) interacts with the channel selection +DS(X) to define an offset which is added to the content of the Address Counter to form the final address. The LSB (+A00/+A07) is not affected by the offset, thus the incrementing of the address counter selects the lower 128 memory locations without modification. The MSB (A08/+A015) is subject to modification. The offset PROMs (U10, and U25) are pre-programmed read-only memory. The content is addressable via the input A0-7. It can be noted that a single base address coupled with the frame size, channel selection, and selection of Zero Insert, can completely define the buffer layout used for DMA operations. The channel offset is derived from the channel index counter (U8). The counter is reset to zero at the start of each Scan (except during CONTINUOUS operations - see Double Buffering). At the completion of each DMA operation (-DMACK) the counter is incremented to reflect the selection of the next channel in the scan. This in turn will change the address presented to the offset PROMs and result in the selection of the corresponding location for that channel's data word.

(5) **Double Buffering.** During Scan operation U8 is initially reset and remains so during the acquisition of the first data buffer. This function permits the first accumulation of data to occur with Channel Index counts of 0_8 through 7_8 depending on the number of channels being sampled. If CONTINUOUS operation is selected (764000, bit 14), data acquisition is to continue on an uninterrupted basis from one frame to the next. In order to keep the data being acquired in the second frame from overlaying the data in the first frame, the Channel Index Counter (U8) will be loaded with the Channel Code +1 on all even numbered data frames. This operation takes place in U4 and is permitted by the inhibiting of the "Clear" input to the Channel Index Counter by U18 Pin 8. Since U18 Pin 8 is simply complemented on the completion of each frame during a CONTINUOUS operation, the Channel Index Counter will alternate between an initial count of zero and the channel code +1.

3.1.8 ADS Digital Control Board No. 2 (2501-4713-2D)

The ADS Digital Board No. 2 consists of the following circuitries: First-In First-Out Buffer, Bus Overload Detection, DMA Data Transfer and Sample Generator. A description of each of the circuits is provided below.

3.1.8.1 First-In First-Out Buffer (FIFO). The 12-bit binary word from the A/D is inverted by U40 and U43 and then presented to a sixteen word ripple storage buffer U39, U41 and U44. The 11-bits data, 1-bit sign and 1-bit over data word waits in the FIFO until a DMA operation moves it into the memory. Writing to the FIFO is accomplished by -OFFCK and reading by U10 pin 10. Address is generated internal of the FIFO chips.

3.1.8.2 DMA Request. Whenever data is entered into the FIFO buffer via the strobe pulse "-OFFCK", U8 Pins 3,4 and 5 sense a word in FIFO and set DMARQST FF U2 Pin 12.

3.1.8.3 DMA Data Transfer. When a DMA request has been made by ADS (-DMARQST) through the Universal Interface, no further action is required by ADS until it is made Bus Master by receipt of "-AMAST". This signal -AMAST with DMA requests (U11 Pin 8) to produce +AGATE and +DBIN. The memory address to which the data in FIFO is to be routed is gated from the DMA Address Register with the appropriate offset (+A01/+A015) through the Universal Interface to the Unibus by +AGATE. It is important to note that "+AGATE" is wired into the Unibus Control Signal "+OC1" while "+OC00" is wired to ground. In accordance with Unibus convention, these signals determine the direction of data movement - in this case a DATO is in progress. This condition will produce "-READ" by inhibiting U35 Pin 6. The Read Write Jumpers at E31/E33 transpose the term "-READ" to "-REDHI" and it is routed back into the ADS logic and inverted (U32 Pin 4). With the address already

issued to the host memory (+AGATE) and the direction of data established (+OC1,+OC0), "+DBIN" (U5 Pin 5) gates the data to the Unibus. While the address and data lines are active, the assertion of Master Sync (-UMSYN) will occur with the setting of U1 Pin 5 and U1 Pin 9 on successive clocks of -4MB. U1 Pin 5 is used to initiate a 16 μsec time-out of master synch via U28. When U1 Pin 5 is set it enables U28 by removing the clear (pin 14) and permitting an advance of the counter every 1 μs. (1 MHz). If Slave Sync is not received within this period of time to signal successful completion of the DMA by resetting U1 Pin 5 (U12 Pin 12), the carry from U28 will clear the DMA request FF.

Note that no indication of this event is visible to the operating software (i.e., no flag is set). However it is obvious that if subsequent DMA's are also unsuccessful or if the sample rate vs. bus availability is tight, a bus overload condition will invariably result (U2-5). The rest of U1 Pin 9 also results in the application of a clock to the FIFO Read U39, U41 and U44, Pin 16 indicating removal of a word from the buffer and selecting the next word in FIFO for UNIBUS transfer.

3.1.8.4 Bus Overload. A Bus Overload condition will occur if the DMA service rate falls below the Data Aquisition Rate to the point where the FIFO buffer is full and another word attempts to pass from the A/D into FIFO. The comparator circuit U8 will produce a positive signal (output pin 8) when the FIFO is full. High sampling rate or very active Unibus operation can slow the ADS DMA servicing to the point where the FIFO becomes full. When this occurs, and another word of data is presented to the FIFO, i.e., another -OFFCK appears, the Bus Overload FF U2 will set. A Bus Overload condition can be averted at the last moment however, if a DMA in progress removes a word from FIFO, i.e., -DONECL U2 Pin 1.

3.1.8.5 Sample Control. The ability of ADS to initiate sampling is determined by the Sample Control Circuit. The +TRIGGERED FF (U62 Pin 5) must be set to enable both the sample timing and sample generator logic. Although +TRIGGERED may be set either by -FREE RUN or by a trigger condition (U61 Pin 6), it must first be enabled by removing a reset (U66 Pin 6). All three of the following conditions must be present to enable +TRIGGERED to be set:

- The ADS unit must be "Sample Enabled" (764000, Bit 4)
  This produces +SAMP EN to U66 Pin 4.
- A -STOP condition must not be present (U61 Pin 8) i.e., not "full buffer" or "transient stop" conditions.
- A "Frame Done" Condition must not exist (U15 Pin 6).

Resetting Sample Enable or the presence of STOP (full buffer) or FRAME DONE will reset +TRIGGERED, inhibiting any further sampling.

3.1.8.6 Sample Generator. The Sample Generator consists of a series of Control FF's U62 and 31, a ripple counter U46 and the Channel Scan Logic (U48,64,65). Additionally the +4MHz clock is applied to the Binary counters at U16 and U17 to produce a 1 MHz 1 μs clock. The primary functions of the Sample Generation Logic are as follows:

- Select the channel to be sampled,
- Issue the "-Hold" command to the Analog Sample Logic, and
- Issue the "Start Convert" Signal to the A/D Logic.

Selection of the channel to be sampled is a function of the Channel Code segment of the Control and Status Register (764000). Bit positions 10-12 determine which channel or channels are to be sampled while bit 9 (+SCAN) defines whether a single channel or a scan of multiple channels is to occur. If a single channel only is to be sampled, the Channel Code is locked into the Channel Scan Counter (U48) by +SCAN. The Channel Selector (U64) will decode the appropriate channel enable (CHAEN through CHHEN) which is sent to the analog multiplexer. Likewise, the Channel Offset selector (U64) will remain static.

During a Scan operation, the Channel Code (CHNL 0/2) defines the last channel in the scan sequence. The operation is initiated with the Channel Scan Counter (U48) at zero. Each time the hold interval Counter (U46) completes its sequence, the channel Scan Counter will be incremented. Note that counter U48 is reinitialized (reset) with each +SAMP and continues coming up with each "hold" sequence until the decode of the Channel Scan Counter is equal to the Channel Code (764000, Bit 10, 11, 12). At that time U49 Pin 3, 11 and 4 will be high producing +SCAN DONE which is applied to (U30 Pin 8) to reset the Start Scan FF (U62 Pin 9). This completes the sequence for Channel selection in a SCAN Mode. Note that a +TRIGGERED condition must exist to provide a set pedestal for the start scan FF (U62 Pin 9).

The "HOLD" sequence is initiated with the arrival of the "+SAMP" signal which sets the Start Scan FF. The next "+1MHz" clock to arrive sets U31 Pin 55 and produces "+HOLD ENABLE". This sequence effectively "ripples" a 1 μs positive pulse through the Hold Interval Counter to produce a 6 μs cycle time. As long as the Scan is in progress (+HOLD ENABLE is active) the counter is self-initiating every 6 μs. The Start Convert Pulse FF (+STCONVP) is generated 250 ns after "-HOLD". It is issued to the A/D converter to initiate the conversion of the Analog Signal to binary format and is 1 μsec in duration.

3.1.9 Trigger Board (Schematic 1923-4982-2D)

The trigger board accepts inputs from four sources: 1,2,3, or external. In the first three cases the full scale range is equal to the full scale setting of the selected channel. For the external input, the range is ±2V. The selected trigger input is level shifted and compared with the output of a 6-bit D/A. This gives 64 possible trigger levels ranging from -F.S. to +F.S. The slope may be +, -, or both (whichever occurs first). The trigger output is also used for transient capture since in that case triggering in the normal sense is impossible.

The ADS may be operated in either a free running or triggered mode as determined by register 764002, bit 11. When free running is selected, +TRIGGERED is held set permitting continuous sampling to occur. However, when triggering is required (-FREERUN), +TRIGGERED FF must be set from U61. Since the trigger source may be based on a selected slope (+TRIG) or a digital trigger input (-DIGTRIG), the state of U26 Q4 is examined. The presence of either bit 15 or 14 during a trigger mode load (764002) defines the slope for an "internal" trigger. The absence of either indicates a digital trigger input from an external source. The objective of the trigger circuits is to produce the signal +TRIG based on:

- **Source** - The analog input from Channels 1-3 and an external input is read into a FET selector at U3 and U5. The enable is derived from a segment of the Trigger Mode Register (764002, bits 12 and 13) decoded through U6. The gated source (TP1) is then presented through level shifter R1/R2 into the Amplifier/Inverter to U1.

- **Level** - The input level to U1 may be biased by the input through R19 (TP2) from the programmable 6 bit D/A precision resistance network R14/R15. The selection of the Bias Level is controlled by U10 (764002, bits 0-5).

- **Slope** - The "selected" and "biased" signal (TP3) is passed through U2 where a zero adjust capability (R18) exists (TP4) and is presented to the positive trigger SS (U4 Pin 4) and the negative trigger SS (U4-12). The appropriate enable is derived from register 764002, bits 14 and 15. The signal produced is a 700 ns +TRIG.

3.1.10 Power Fail Detection

Two diodes have been added in series to the AC LOW and DC LOW (BF1 and BF2 of the backplane) for power fail detection. These diodes are soldered between the power supply harness and wire wrap to BF1 and BF2. Heat shrink tubing insulates the solder connections and diodes from the backplane pins. The presence of these diodes is not obvious unless the heat shrink is cut to expose the components.

SECTION 2

Q-BUS DIGITAL-TO-ANALOG SUBSYSTEM

3.2.1 Introduction

The following text is primarily referenced to the Q-DAS Schematic 2510-4701-2D which is located in the System Reference Volume 2511-0103.

The Q-Bus Digital-to-Analog Subsystem (Q-DAS) is used in the 2511/2514 Vibration Control Systems to generate an analog output signal which is used to drive shaker tables. The Q-DAS is somewhat like a single channel ADS in reverse consisting of a direct memory Q-Bus interface for reading digital data blocks from memory, a 12-bit digital-to-analog converter, output smoothing filters and a programmable attenuator to adjust the final output level (see Figure 3-2). The Q-DAS is automatically progammed through the test setup specifications of the vibration and shock control programs.

3.2.2 Q-DAS Registers and Bit Assignments

The address assignments of the Q-DAS registers are as follows:

Register Address	Function
764300	DMA Address Register
764304	Control Status Register
764306	DMA Word Counter
764310	DAC Holding
764312	Attenuator Holding
764314	Filter Codes
764316	Multiplexing

Figure 3-3 summarizes the Q-DAS registers and functions. The following paragraphs describe the various registers and bits individually.

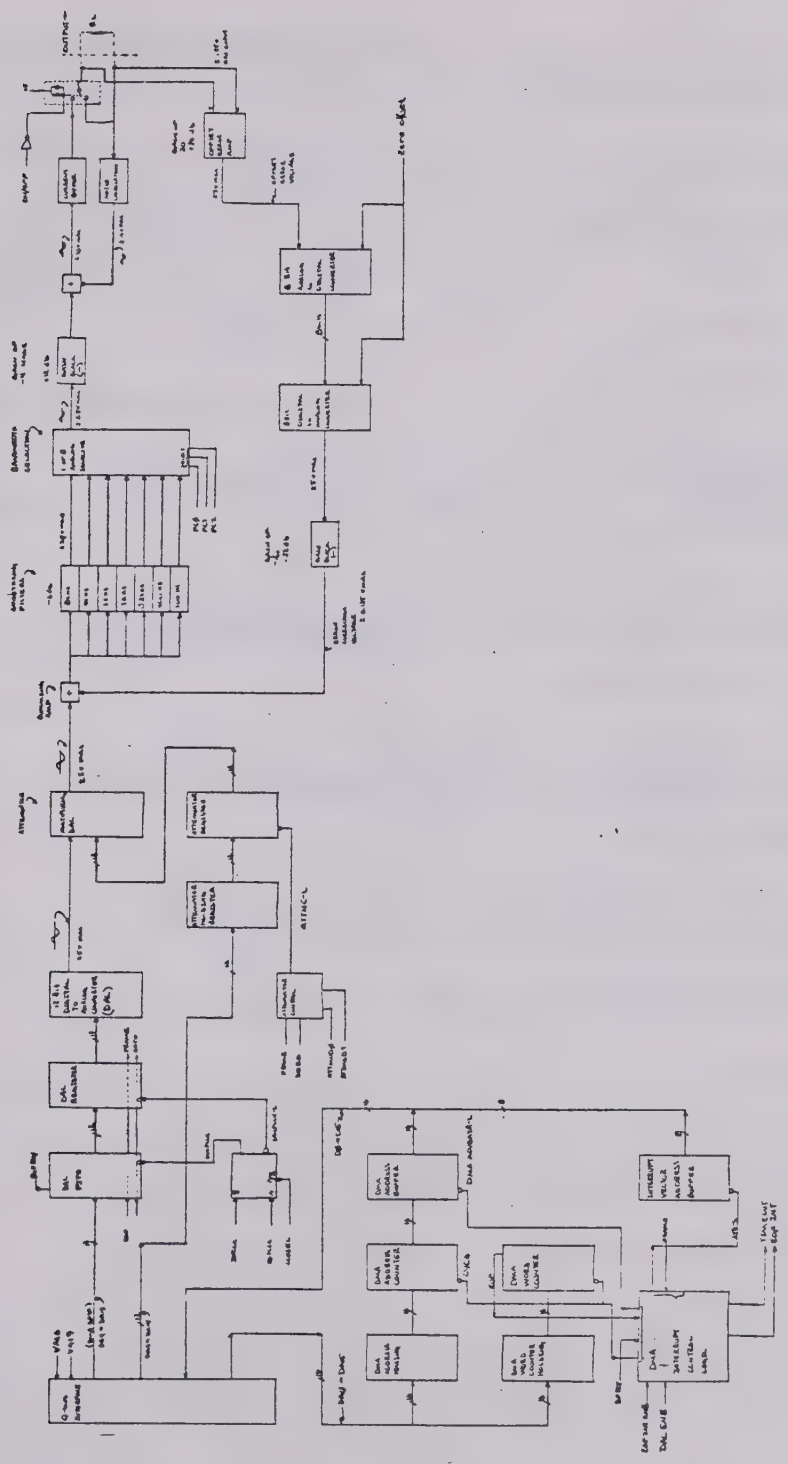


Figure 3-2. Q-DAS Block Diagram

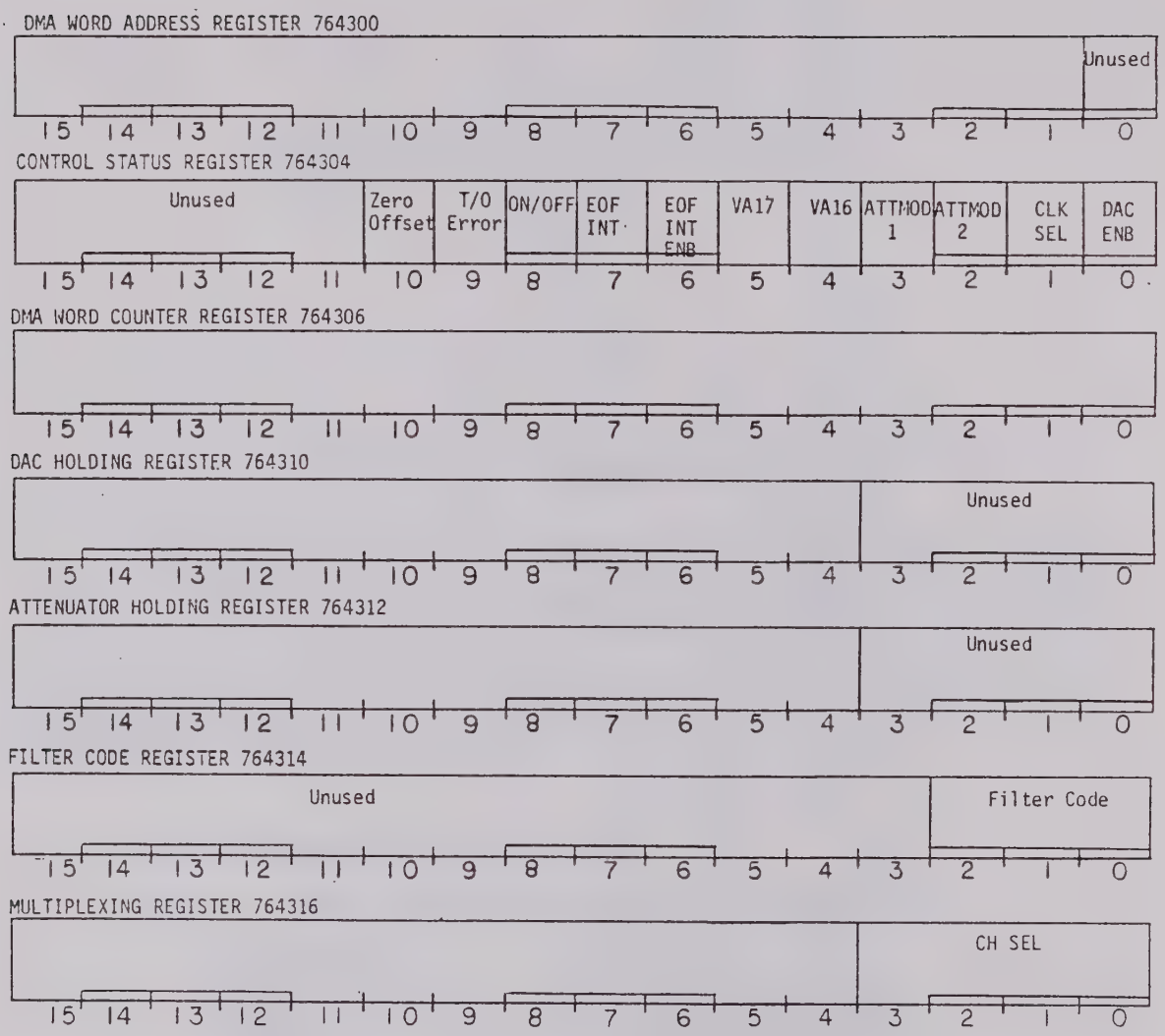
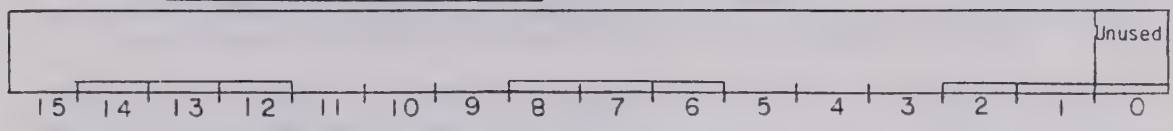

DMA WORD ADDRESS REGISTER 764300
Unused
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
CONTROL STATUS REGISTER 764304
Unused
Zero Offset
T/O Error
ON/OFF
EOF INT
EOF INT ENB
VA17
VA16
ATTMOD 1
ATTMOD 2
CLK SEL
DAC ENB
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DMA WORD COUNTER REGISTER 764306
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
DAC HOLDING REGISTER 764310
Unused
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
ATTENUATOR HOLDING REGISTER 764312
Unused
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
FILTER CODE REGISTER 764314
Unused
Filter Code
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0
MULTIPLEXING REGISTER 764316
CH SEL
15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

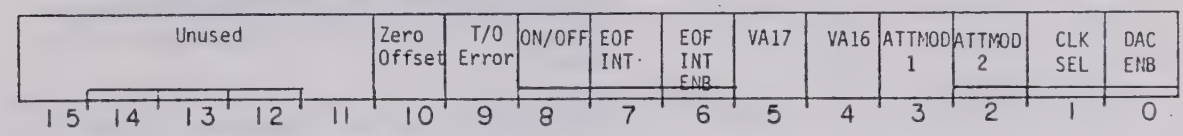
Figure 3-3. Q-DAS Control Registers

3.2.2.1 DMA Word Address Register (764300)



The DMA Word Address register is loaded under program control with the starting address of the next DMA operation.

3.2.2.2 Control Status Register (764304)



ZERO OFFSET — This bit, when set, enables the zero offset circuitry to zero the output of the Q-DAS by compensating for any affects in the filter blocks chosen.

T/0 ERROR — This bit is set when the Q-DAS output detects an error in the DMA channel. This error is caused when a load of the DAC is attempted and the DMA data is not present.

ON/OFF — This bit, when set, enables the Q-DAS drive section. When cleared, this bit disables the Q-DAS drive section.

EOF INT — When set, this bit signifies that an end of frame has occured.

EOF INT ENB — When set, this bit enables the interrupt on end of frame (E OF INT). When cleared, this bit disables the E OF INT.

INPUT LEVEL — These bits select the DAC input level +FULL SCALE to -FULL SCALE as follows:

```
011111111   111 = +FULL SCALE (+10V)
000000000   000 = ZERO (0V)
100000000   000 = -FULLSCALE (-10V
```

VA17 & VA16 — When these bits are set, they allow DMA Word Address register to extend its addressing range to 128 K words.

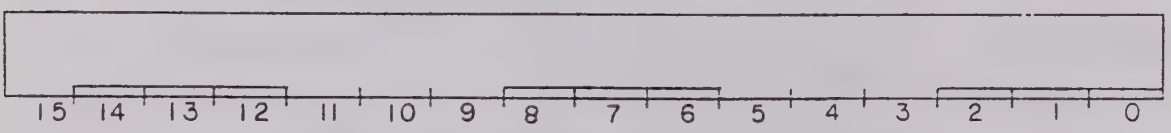
ATTMOD 1,0 — These two bits define the loading mode for the Attenuator register from the Attenuator Holding registers as follows:

00	Load synchronously with next loading of the Attenuator Holding register. This is also the mode that is forced during a hardware reset. After a hardware reset, the attenuator loading mode must be selected under program control.
01	Not used, reserved for future expansion
10	This mode forces the Attenuator register to be loaded at the end of the current output frame (EOF).
11	This mode forces the Attenuator register to be loaded from the Attenuator Holding register, when the output of the DAC crosses zero.

CLK SEL — When this bit is set, the Q-DAS internal sample clock is enabled. This internal clock has a frequency of 20, 480 Hz. When CLK SEL is cleared, the external sample clock is used as the Q-DAS sample clock. On the 2511/2514 system, this external clock is usually the ADS clock.

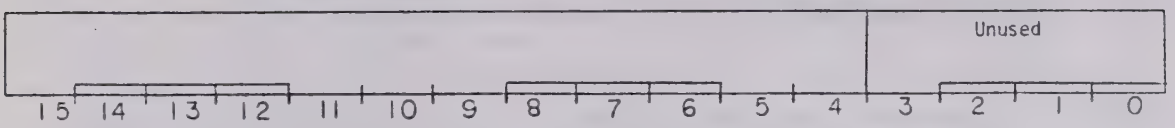
DAC ENB — When this bit is set, it enables the Q-DAS to DMA from Q-bus memory. When this bit is cleared, the DMA channel is closed. If the DAC END bit is cleared in the middle of an output frame, the current output frame will continue, along with DMA, until the end of frame (EOF) occurs.

3.2.2.3 DMA Word Counter Register (764306)



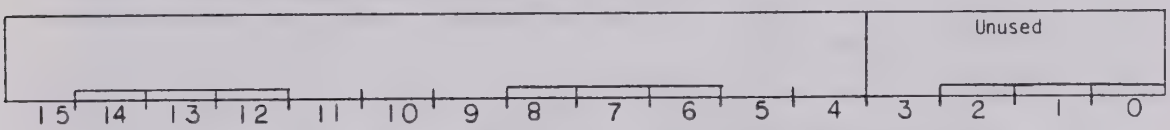
The DMA Word Counter consists of a holding register (U45, U57) which is loaded under program control and an up/down counter (U30, U44, U56, U72). The data in the holding register is clocked into the up/down counter at either end of frame (EOF) or immediately when the DAC ENB bit (bit zero of the Status and Control register) is cleared. This register serves to hold the number of words minus one that the DMA Word Address register is currently pointing to (i.e., the number of words in the buffer for DMA transfers). Since the number of bits is limited to 16, this places an upper limit on the length of the buffer that can be output through the Q-DAS of 65,535 (decimal).

3.2.2.4 DAC Holding Register (764310)



The DAC Holding register (U47, U48, U49) is actually a 16 word FIFO which is loaded under program or DMA transfer control. A FIFO was used so that the Q-DAS could run without a DMA channel for up to 16 clock counts without introducing discontinuities in the output.

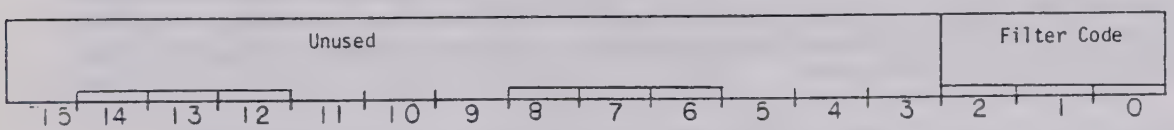
3.2.2.5 Attenuator Holding Register (764312)



The Attenuator Holding register consists of a holding register (U77, U91) which is loaded under program control with the next attenuator setting to be loaded into the attenuator) and a buffer register (U76, U60) which is loaded from the holding register according bits 2 and 3 of the Control Status register as follows:

00	This mode forces the Attenuator Register to synchronously with the Attenuator Holding register.
01	Not used, reserved for future expansion.
10	This mode forces the Attenuator register to be loaded at the end of the current output frame (EOF).
11	This mode forces the Attenuator register to be loaded from the Attenuator Holding register whenever the output of the DAC section crosses zero.

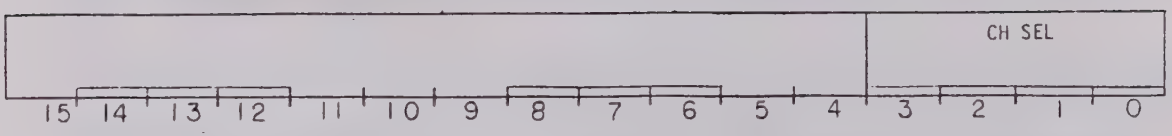
3.2.2.6 Filter Code Register (764314)



This register is loaded with a three-bit code used to select one of the seven filters available on the Q-DAS.

Bits	Frequency
000	0 to 200 Hz
001	0 to 500 Hz
010	0 to 1000 Hz
011	0 to 2000 Hz
100	0 to 2000 Hz
101	0 to 8000 Hz
110	0 to 3000 Hz
111	AC level of 0 volts

3.2.2.7 Multiplexing Register (764316)



This register is only used in conjunction with optional 16-channel selector.

CHSEL — These bits determine which channel is to be read from the optional 16 channel selector to the ADS.

Bits	Channel
1111	1
1110	2
1101	3
1100	4
1011	5
1010	6
1001	7
1000	8
0111	9
0110	10
0101	11
0100	12
0011	13
0010	14
0001	15
0000	16

3.2.3 Q-DAS Board (Schematic 2510-0701-2D)

The Q-DAS board consists of the following circuitry: Q-DAS Interface, Read/Write Logic, Q-DAS Interrupt, DMA Logic, DAC Holding Register, Attenuator Holding Register, Multiplying DAC, and Zero Offset. A description of each circuit is provided below.

3.2.3.1 Q-Bus Interface. The bidirectional data bus (Q-bus) BDAL0-BDAL17 is buffered onto the Q-DAS with U95, 94, 93 and 100. Note that U100 also buffers the BBS7 line which On assertion indicates use of the I/O page in memory. On the Q-Das, the bidirectional data bus BDAL0-BDAL17 is divided into two functional groups, D16 & 17 and D0-D15. D16 and D17 are used in conjunction with the Status Control register bits VA16 and VA17 which allows the Q-DAS to extend its memory addressing range to 128K words. D0-D15 are used as an internal output bus that serves the following:

- The DMA section as the low 16 bit of output address
- The Q-Bus read function to read the status of the Status Control register.
- Serves as the internal input bus to bus information from the Q-bus to the registers on the Q-DAS.

U98 and U99 are used to buffer bidirectional control lines, while U97 buffers input only control lines. Jumpers J1-J9 form the bus address of the Q-DAS board (764300 octal) which is compared to the address on the Q-bus during any read/write operation. This comparison of the jumpered address and the Q-bus address takes place in U62 and U63. The output of this comparison is DEVSEL. If the comparison yields an address within the Q-DAS register page, DEVSEL is asserted. If the address is not within the Q-DAS register page, DEVSEL is negated, and no other operation is performed. Jumpers J1-J8 are selected by either wiring in the jumper giving a logical 0 or leaving the jumper out giving a logical 1. Jumper J9 when wired from A to B gives a logical 0, and when wired from A to C gives a logical 1.

3.2.3.2 Read/Write Operation.

NOTE

The only readable register on the Q-DAS board is the Control Status register; all other registers return a value of 177777 (octal) to the program when read.

A read operation is initiated when the DEVSEL line is asserted. When the DEVSEL line is asserted, a 4-bit code is clocked into U96. Three of the 4-bits are then used to drive U50, a one of eight decoder that selects the register to be read. When the processor is ready to accept data, it assets the BDIN line. The assertion of the DBIN line causes the data in the register being read to be placed onto the internal data bus (D0-D15) and then along with DEVSEL passes the data to the Q bus (bidirectional data lines BDAL0 through BDAL15). At this time the Q-DAS, using BDIN as a guide, passes a BRPLY to the processor to acknowledge the data as being valid. The processor then clocks in the data and negates the BDIN line. This causes the Q-DAS to negate BRPLY ending the bus cycle.

A write operation is initiated when the DEVSEL line is asserted. When the DEVSEL line is asserted, a 4-bit code is clocked into U96. Three of the four bits are used to drive U50, a one of eight decoder that selects the register to be written to and readies it to accept data from the Q bus (which is always active on data lines DA0 through DA15). When the processor has valid data on the Q bus, it asserts the BDOUT line. The BDOUT Line is then used as a model for the BRPLY Line which is asserted by the Q-DAS. When then processor detects the assertion of the BRPLY Line it negates the BDOUT Line. The edge produced by negation of the BDOUT Line is used to clock the data from the Q-bus into the addressed register. The negation of the BDOUT line also causes the negation of the BRPLY Line thus signaling the processor that the bus cycle should end.

3.2.3.3 Q-DAS Interrupt Cycle. An interrupt cycle starts in the DMA section when the DMA WORD COUNTER runs out and produces a pulse called end of frame (EOF). This EOF pulse is passed through the DAC Holding Register and is called FRAME. When FRAME occurs, FF U81 is set. This output is fed to the Control Status Register as EOF INT and is used to signal the driving program that an interrupt condition has occured. The rising edge of FRAME clocks flip flop (FF) U51. If EOF INT ENB is asserted, then this assertion is passed through FF U41 and signals an internal state of interrupt pending. This interrupt pending state lasts until BIRQ6, BIRQ5 and BIRQ4 are all negated, indicating that there are no other device interrupts to the processor. As soon as there are no other interrupts, U84 is clocked to produce an interrupt request on BIRQ4 at the termination of the current bus cycle, as indicated by BSYNC. When this occurs, INT REQ is asserted, which clears the interrupt pending state in FF U41, and is passed onto the Q bus as BIRQ4. In this state, the Q-DAS is waiting for the processor to acknowledge an interrupt condition. This happens when the processor asserts BDIN while BSYNC is negated, indicating a non-memory Q bus cycle. This is also the time that all devices requesting an interrupt must arbitrate to see who gets to be serviced first. Arbitration is won by being the device that can receive BIAKI and block BIAK0 to another deivce. In the Q-DAS, this is done by using BDIN with BSYNC-L to clock FF U84, creating a signal that blocks out BIAK0. This signal also negates the INT REQ signal, and hence, the BIRQ4 Q bus signal. After this, the Q-DAS waits for BIAKI to be asserted, indicating that the interrupt vector should be passed to the processor, along with a BRPLY to acknowledge the transfer. The interrupt vector is enabled to the Q bus by the assertion of interrupt vector data (IVD). IVD is made up of the signal from FF U84 (that blocks BIAK0) and BIAKI, and is used by the Q-DAS to allow the interrupt vector address to be placed on the Q bus. BIAKI is also used as a model for BRPLY that is sent back to the processor to acknowledge the interrupt vector transfer. After the interrupt vector transfer is complete (IVD negated), FF U84 is cleared and the Q-DAS interrupt secton waits for another interrupt. The interrupt vector address of the Q-DAS is 360 (octal).

3.2.3.4 DMA Cycle. A DMA cycle is initiated when the DAC ENB bit (bit zero) from the Control Status Register is set and the input ready (BUF REY) line from the DAC Holding register is asserted. BUF RDY along with EREN and BDMGI are clocked into flip-flop U54 which produces the signal VDMA REQ and the Q-bus signal BDMR. When BDMR is asserted the sequential state machine, composed of U39, U40, U25 and parts of U26 take over. The first act of this machine is to monitor the Q-bus BDMGI line. When BDMGI is asserted, the machine asserts DMA ACK the DMA AD/DAS signal is then asserted, which allows the output from the DMA Address Counter (U74, U73, U89 and U88) to be passed onto the Q bus as address information. After this address information has been on the Q-bus for the required address setup time, the DMA SYN signal (the Q bus signal BSYNC) is asserted which starts a Q bus memory cycle. The DMA AD/DAT signal is then negated, and the signal DMA DIN is asserted. DMA DIN is passed to the Q bus as BOIN and is used to signal the memory that a read operation is in progress. At this time the machine waits for BRPLY to be asserted, indicating that the output of the addressed memory location is valid. When this occurs, the machine asserts the signal CYC6. When CYC6 is asserted, it allows the following events to occur:

- The memory that was accessed is loaded into the DAC Holding Register.
- The DMA Address Counter is incremented, so that on the next cycle, the Q-DAS will be pointing to the proper memory location.
- The DMA Word counter is decremented so that the DMA section can keep tract of how much of the buffer has been outputed. Specifically, it allows the DMA section to know when it finishes outputting any specific buffer.

The context of EOF is saved along with the DMA data on CYC6. However, EOF is not updated at flip-flop U23 until the data from the DMA Address Counter has been used as address information to the memory and the DMA Word Counter has been decremented. This insures that the last word in the Buffer which will be output before the DMA Word counter and DMA Address Counter are reloaded.

NOTE

When DAC ENB is negated, EREN will not be negated until the end of frame EOF.

3.2.3.5 DAC Holding Register. The DAC Holding register (U47, U49, U48), a 16 word FIFO, is loaded under program or DMA transfer control. The FIFO produces two control signals, BUF RDY and TIMEOUT that reflect the status of the FIFO. When BUF RDY is asserted, it indicates to the DMA section that the FIFO has an open location for new data. This causes the DMA section to initiate a DMA cycle (as described above) to get another data word from the output buffer in memory. This word is accessed from memory, and clocked into the FIFO when signal CYC6 is asserted. Data is unloaded from the FIFO on the positive edge of SAMPCLK and loaded into the DAC register on the negative edge of SAMPCLK.

A timeout error occurs (TIMEOUT asserted) when the flow of data through the FIFO is restricted for more than 16 samples. If a new word is loaded into the FIFO before the 17th output is attempted, the Q-DAS will recover without a time out error occuring. If a timeout error does occur, the Q-DAS will not manufacture any missing states, nor any erronous data points. It will set quietly, its output equal to the last data point, until the DMA channel reopens.

3.2.3.6 Attenuator Holding Register. The Attenuator Holding register consists of a holding register (U77 and U91) which is loaded under program control and a buffer register (U76 and U60) which is loaded from the holding register according to bits 3 and 2 of the Control Status register as follows:

ATTMOD1	ATTMOD0	
0	0	Loaded synchronously with the holding register (U77 and U91)
0	1	Not used, reserved for future expansion
1	0	Loaded at the end of the current output frame (Frame Asserted).
1	1	Loaded whenever the output of the DAC Holding register crosses zero. A zero crossing is detected by comparing the sign of the current output word to the sign bit of the last output word. This transition is detected by U29 and is brought the DAC section as ZERO. The delay of the sign bit for the previous output word is provided by flip-flop U46.

3.2.3.7 Multipying Digital to Analog Converter. The signal from the Multiplying Digital to Analog Converter (MDAC), a 10 V peak to peak signal, is summed to a zero offset voltage (refer to paragraph 3.2.3.8) through an op-amp in U43. After this summation with the zero offset voltage, the analog signal is passed to the inputs of all 7 of the smoothing filters. This selection of which filter is to be used is accomplished by U71, a 1 of 8 selector. The output of U71 is passed to U22 a high impedance gain of 2 op-amp. This gain of 2 is needed to reestablish the original signal level from the MDAC, because each of the filters has a gain of 1/2. Since the final drive signal level is a 20 V peak to peak signal, the filter output is again put through U22 to boost the signal up to its full level. This signal is then passed to the summing junction U22 pin 9 where noise on the drive signal return line is summed into the drive signal. The purpose of the summing junction is to add the noise on the drive signal return line to the drive signal itself, so that the absolute difference between the drive signal and its return line is always what was set at the DAC. The signal then passes through the high current output buffer U27 and is routed to relay K1. Relay K1 is used to turn the drive signal ON and OFF, passing the drive signal through when the relay is active, and passing the drive signal return through when it is inactive.

3.2.3.8 Zero Offset. The zero offset circuitry is used to compensate for offsets that occur inside each of the filtering elements. Before the zero offset circuitry can be enabled, the following conditons must be met. The output of the DAC section must be set to zero, the filter to be used must be selected, and the relay (K1) that controls the Q-DAS output must be ON. When all of these conditions are met, the Zero Offset bit in the Control Satus register is set and the zero offset circuitry is enabled.

The digital outputs of the 8-bit analog to digital conveter U86 are tri-stated. This allows the pull-up and pull-down resistors on the outpus to push the outputs to a state that gives a zero volt reading to the inputs of the 8-bit digital-to-analog converter U87, which proceeds to output an analog signal of zero volts. This zero volt signal is then summed into U43 as the zero offset voltage and the filter that is being calibrated is isolated. This isolation is due to the fact that the DAC is outputting zero, the zero offset section is ouputting zero, so the only thing in the loop that can be putting out an offset is the filter block and/or drive section. The offset due to the filter block and/or drive section is reflected in the absolute difference between the output voltage of the drive section and its return line. The difference of the drive section and its return line is measured (±5 volts max) and presented to the U86 during the 500 ms period that the zero offset bit is asserted. The outputs of U86 are held inactive until the zero offset bit is negated. When the zero offset bit is negated, the zero offset section sums the exact opposite of the measured difference, divided by 2, into the summing junction U43. This effectively cancels the offset due to the filter block and/or drive section. The maximum offset adjustment that this section is capable of is ±0.25 volts.

SECTION 3

GR2501 MICROPROCESSOR

The 2501 microprocessor consists of the following major components, which are described in this section:

Backplane	2511-2014	(Bus Structure)
CPU Board	2501-4700	(Processor)
PROM Board	2501-4701	(Instruction Menu and Misc)
Display Board	2501-4702	
Unibus Interface Board	2501-4703	

3.3.1 2501 Bus Description

3.3.1.1 General. The following text is primarily referenced to the diagrams listed below:

Backplane	2511-2014-4D, 8D
CPU Board	2501-4700-2D
PROM Board	2501-4701-2D
Display Board	2501-4702-2D
Unibus Interface Board	2501-4703-2D

The microprocessor bus is a synchronous bus. This distinguishes it from an asynchronous, or handshaking type of bus. Everything on the microprocessor bus is done at a time relative to the master clock, a clock pulse which occurs once every microprocessor bus cycle (every 250 ns to 1000 ns). The bus cycle and the microprocessor instruction cycle are always an integral number of 62.5 ns clock pulses in length. The microprocessor bus serves to perform the following three major functions:

- Data transfers (16 bit word) can be done from one bus device to another as commanded by the microprocessor. A source device is selected by the source field in the microinstruction and a destination device is selected by the destination field in the microinstruction. The source and destination devices decode their selection during the microinstruction prior to the microinstruction in which the data transfer will take place. Readout of microinstructions is always one instruction cycle ahead of the execution of the microinstruction. The source device will put the data on the bus at the beginning of the instruction cycle and will hold the data on the bus for the duration of the instruction cycle. At the end of the insruction cycle the destination device will receive the data, generally by clocking it into a register with the trailing edge of the master clock pulse.

- The second major function of the microprocessor bus is to provide a means by which devices on the bus may cause an interrupt in the microprocessor. The device first makes an interrupt request at one of 7 levels of priority by enabling one of 7 interrupt request lines. The interrupt request lines are open collector ORed. More than one device can request an interrupt on the same line at the same time. When priorities permit, the microprocessor enables one of 7 interrupt grant lines. The interrupt grant lines are chained so that only the first requestor on an interrupt grant line sees the grant. On the cycle following the grant the remote device enables 8 interrupt vector lines to specify to the microprocessor the address of the interrupt vector in the microprocessor's control store. The microprocessor will then be interrupted, executing the instruction stored at the interrupt vector location and saving its return address in the program interrupted.

- The third major function of the microprocessor bus is to provide a means for a remote device to signal its condition to the microprocessor. The condition is either true or false and the microprocessor jump instructions are controlled by the state of the condition. Thus the microprocessor can do conditional jumps depending upon a condition signaled by a remote device on its bus. The condition is signaled by a single line, the condition true line. The device which is to send its condition is selected by the source field (also called the condition field) of the microinstruction.

3.3.1.2 Bus Line Signal Names and Functions.

DB0	(C2J)	Data lines, 16-bit, least significant.
DB1	(C1K)	
DB2	(C2K)	
DB3	(C1L)	
DB4	(C2L)	
DB5	(C1M)	
DB6	(C2M)	
DB7	(C1N)	
DB8	(C2N)	
DB9	(C1P)	
DB10	(C2P)	
DB11	(C1R)	
DB12	(C2R)	
DB13	(C1S)	
DB14	(C2S)	
DB15	(C2T)	Data lines, 16-bit, most significant.
OSCOUT	(C1A)	16 MHz oscillator (transmission line). Master clock. It is a negative going pulse of length 62.5 ns which repeats with a period between 250 ns and 1000 ns, depending upon the microinstruction being executed (trans-mission line).
CNDTRU	(C2D)	Condition true line. Used to signal a condition from a remote device selected by the source field to the microprocessor. This is a tri-state line. The microprocessor jump instructions, jump or not jump depending on the condition signaled. The polarity of the condition is arbitrary, since the software can reverse the sense of the jump. Design capacitance is 200 pf.

INITL	(C1D)	Initialize line. When held low for a few μs it resets the microprocessor and other deivces connected to the system. The master clock (MCOUT) does not stop while this line is held low. In the 2501 system the initialize signal is drive from the Unibus interface board. The pulse is about 15 μs long and is derived from the computer Unibus initialize pulse. This line is open collector, with a pullup on the microprocessor board. Thus it may be driven from different locations. When the initialize ends, the microprocessor starts executing the instruction at location zero in the control store.

The following six lines are used to control the period of the master clock. The master clock has a period which is an integral number of 62.5 ns clocks. It can never be less than 4 clocks, or 50 ns. For the purpose of computing the actual period the period is considered to be 2 clocks long and additional clocks are added depending upon which of the six lines are pulled low. If the total number of clocks thus computed is 4 or less, the period will be 4 clocks. If it is greater than 4, then the period will be the number of clocks computed. The SCM lines are for the use of a device sourcing to the data bus and they have values of 1, 2 and 4 clocks. Three other lines are for the use of the destination device and also have values in binary steps. The most clocks that can be added are 7 for the source and 7 for the destination, which added to the 2 base clocks, make a maximum period of 16 clocks, or 1 μs. These lines are open collector and the design capacitance is 200 pf.

SCMO	(C2E)	Add 1 clock for source device
SCM1	(C1F)	Add 2 clocks for source device
SCM2	(C2F)	Add 4 clocks for source device
DCM0	(C1H)	Add 1 clock for destination device
DCM1	(C2H)	Add 2 clocks for destination device
DCM2	(C1J)	Add 4 clocks for destination device

The following 18 lines are the source and destination lines. They are tri-state and come directly from the control store ROM outputs.

S0	(D1A)	Source, least significant.
S1	(D1B)	
S2	(D2B)	
S3	(D1C)	
S4	(D1D0	
S5	(D2D)	
S6	(D1E)	
S7	(D2E)	
S8	(D1F)	Source, most significant
D0	(D2F)	Destination, least significant
D1	(D1H)	
D2	(D2H)	
D3	(D1J)	
D4	(D2J)	
D5	(D1K)	
D6	(D2K)	
D7	(D1L)	
D8	(D2L)	Destination, most significant

The following 8 lines are the interrupt vector lines. They are tri-state. They are used by a remote device to specify the address of the interrupt vector in the control store.

IV0	(D1M)	Interrupt vector, least significant
IV1	(D2M)	
IV2	(D1N)	
IV3	(D2N)	
IV4	(D2P)	
IV5	(D2P)	
IV6	(D1R)	
IV7	(D2R)	Interrupt vector, most significant

The following 7 lines are the interrupt request lines. They are open collector and are pulled low by a remote device to request an interrupt. 7 is the highest priority, 1 the lowest.

IR1	(D1S)	Interrupt request, lowest priority
IR2	(D2T)	
IR3	(D2V)	
IR4	(D2V)	
IR5	(E1B)	
IR6	(E1C)	
IR7	(E2D)	Interrupt request, highest priority

The following 14 lines are the interrupt grant lines in and out. Each board passes the interrupt grant from the in to the out pin, unless it is using the grant. These are totem pole lines.

IB1in	(F1A)	Lowest priority grant in
IG1out	(F1B)	Lowest priority grant out
IG2in	(F1C)	
IG2out	(F1D)	
IG3in	(F1E)	
IG3out	(F1F)	
IG4in	(F1H)	
IG4out	(F1J)	
IG5in	(F2B)	
IG5out	(F2D)	
IG6in	(F2E)	
IG6out	(F2F)	
IG7in	(F2H)	Highest priority grant in
IG7out	(F2J)	Highest priority grant out

3.3.1.3 Bus Line Electrical Characteristics. There are four types of lines used: 1) tri-state, 2) open collector, 3) transmission line, and 4) totem pole, or regular TTL output.

Tri-state lines are used for the transmission of data. Generally a tri-state driver will enable the line at some time following the clock and the receiving component will take the data from the bus at the next clock edge. The important characteristic for these lines are the enable and disable times of the driver and the bus charge time. The bus is thought of as a lump capacitance which must be charged by the driver. The actual situation is more complicated, a weakly driven transmission line with multiple reflections, but a lumped capacitance model is used as an approximation.

Open collector lines are used where an ORing of several different drives is desired, as in the interrupt request lines, or where the slow rise time of open collector lines can be tolerated, as in the master clock delay control lines. The open collector lines have a 390 ohm pullup resistor and are to be driven by an S03 or by an LS125 with the input wired to the enable.

Transmission lines are used for only two lines, the master clock (-MCOUT) and the 16 MHz oscillator (OSCOUT). These lines are driven by an S140 50-ohm line driver located on the microprocessor board. Unless the total backplane length is very short these lines must have a controlled impedance and very short stubs leading from the bus to boards. The line could be a 100 ohm line terminated with a 100 ohm resistor on the backplane or the last board on the line, or if the line runs in both directions there could be a 100 ohm resistor at both ends, fully utilizing the 50 ohm drive capability. The master clock is a transmission line to minimize clock skew and to prevent ringing. The OSCOUT line is transmission line to prevent ringing and preserve pulse shape.

Totem pole, or regular TTL outout is used for lines where there is no common bussing and moderate speed requirements. This includes the interrupt grants, which are chained, and a few other lines.

3.3.2 Processor Description

The following text is primarily referenced to the diagrams listed below:

Block Diagram	Figure 3-4
CPU Board Schematic	2501-4700-2D
PROM Board Schematic	2501-4701-2D

3.3.2.1 General. The microprocessor is a special purpose, high speed computer constructed from approximately 140 integrated circuits. The microprocessor has 32-bit wide instruction paths and 16-bit wide data paths. The instructions are normally stored in PROM. The microprocessor is driven by a 16 MHz clock. A typical instruction takes 300 nanoseconds to execute.

What is part of the microprocessor and what is a peripheral device is not a clearly drawn line, since registers which are a part of a peripheral act much the same as registers considered a part of the microprocessor. Thus the choice made here is slightly arbitrary. The microprocessor, as defined here, physically is located on two printed circuit boards, the CPU (2501-4700) board and the PROM (2501-4701) board. Everything on the CPU board is considered part of the microprocessor, while only a part of the PROM board is part of the microprocessor. The rest of the PROM board contains the fractional multiplier, real time clock and printer interface, which are considered peripheral devices and are documented in section 3.3.3 of this manual.

Additional devices can be interfaced to the microprocessor by the use of the general purpose, high speed microprocessor bus. Included as a part of this bus is a 16-bit data bus used for transferring data within the microprocessor and to external devices. A 9-bit source field and a 9-bit destination field signal various units on the data bus to either supply data to the bus or to receive data from the bus. Data transfers and most bus activity is synchronous with the master clock, a clock pulse which comes at the end of each microprocessor instruction executed. Bus devices can interrupt the microprocessor via seven interrupt request lines and seven interrupt grant lines. The bus device transmits the address where the interrupt is to occur by means of the 8-bit interrupt vector bus.

The microprocessor has a dedicated hardware stack, 16 levels deep, used to implement subroutine calls, returns, and interrupts. The current instruction counter and priority level values are stored on this stack during the execution of an interrupt or subroutine. The values are then restored from the stack at the completion of the subroutine or interrupt servicing routine.

Conditional jumps, subroutine calls and returns can be executed by the microprocessor. The condition tested is either an internal condition (status register) or a condition signaled by an external device connected to the microprocessor bus. The device whose condition is being tested is selected by means of a code on the 9-bit source bus, which also serves as a condition select bus.

The basic arithmetic capability of the microprocessor is contained within a 4-chip, LSI arithmetic unit (Am2901). A 256 word memory, addressable in several modes, is used to provide a fast storage supplement to that included in the Am2901 unit.

An 8-bit map register implements a multiway jump capability and provides a method of swapping data bytes on the 16-bit data bus. The map register also has special hardware which aids in the normalization operation of floating point arithmetic.

The results of the Am 2901 unit's operations set flags in the 8-bit status register. The status register bits can then be fed back into the Am 2901 by certain shift operations or tested by conditional jump instructions.

3.3.2.2 Microprocessor Basic Instruction Formats. The five basic types of instruction formats are:

- Jump (Type 1)
- JSR (Type 2)
- Conditional return (Type 3)
- Immediate data (Type 4)
- General Operation (Type 5)

Jump, JSR and conditional return (Types 1, 2 and 3) are change of control type instructions which are conditional based on the code specified in the 9-bit source/condition field. If the condition test is not passed, the next sequential instruction is executed. If the condition test is passed jump (Type 1) and JSR (Type 2) instructions result in a jump to the address specified in the 16-bit jump target field. For conditional return (Type 3), a return is executed if the condition test is passed. The return is made to the last address stored in the subroutine stack by either a JSR (Type 2) instruction or an interrupt.

The immediate data (Type 4) instruction sources data from the instruction itself to the data bus. The data is accepted by bus destination specified in the 9-bit destination field.

The general operation (Type 5) instruction is where both a source and destination on the data bus are specified by the respective 9-bit source and destination fields in the instruction. The source device selected will put data on the bus and the destination device will accept the data. Variations of the code in the source and destination fields generally cause the more complicated arithmetic functions to take place.

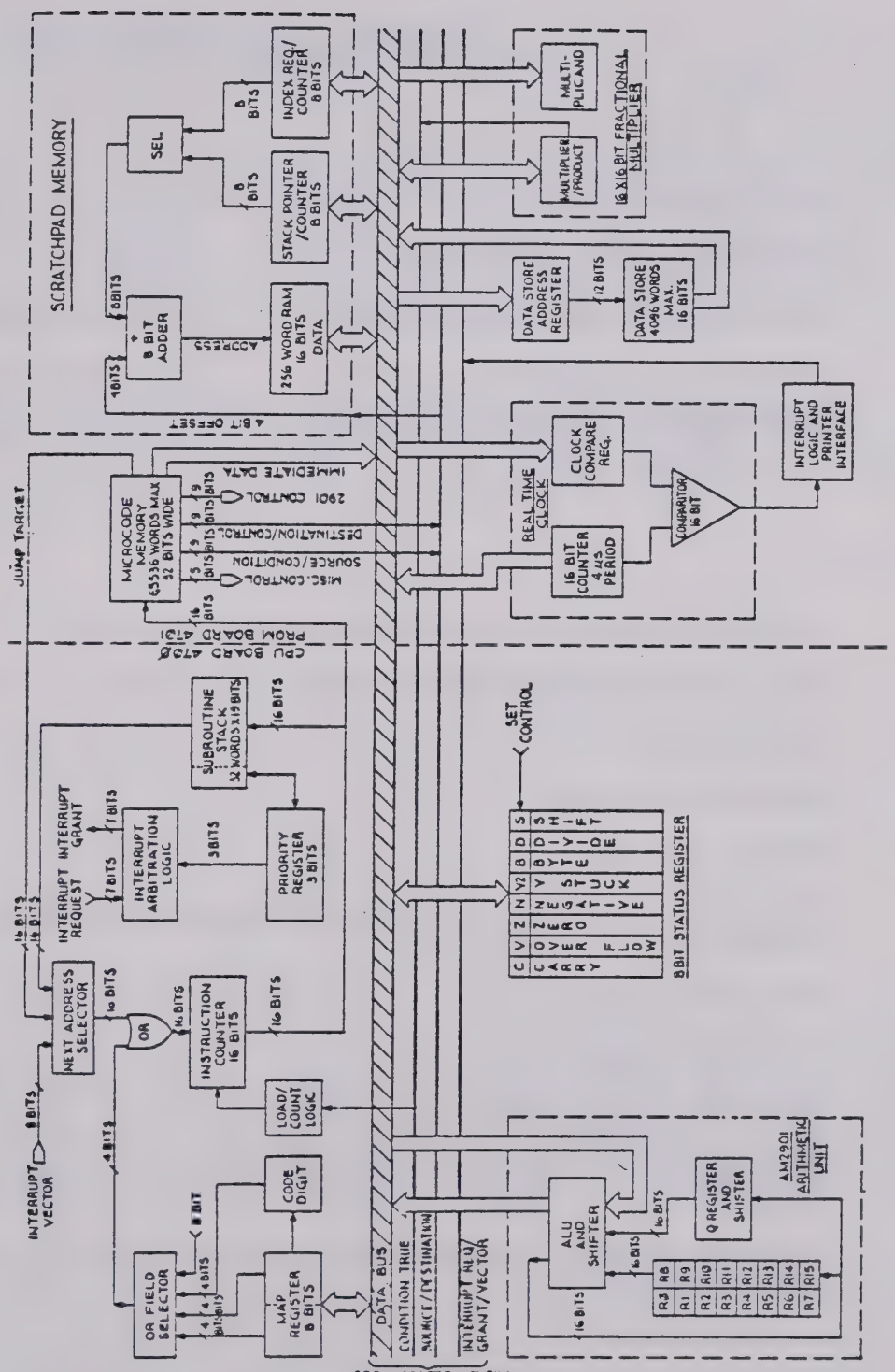


Figure 3-4. Processor Block Diagram (CPU and PROM)

BASIC INSTRUCTION FORMATS

```
 30  26  22  18  14  10   6   2
J00EXCCCCCCCCC00TTTTTTTTTTTTTTTT      Type (1) Jump
J10EXCCCCCCCCC00TTTTTTTTTTTTTTTT      Type (2) JSR
J01EXCCCCCCCCC00XXXXXXXXXXXXXXXX      Type (3) Conditional Return
01REX00IIIIIIIDDDDDDDDDIIIIIIIII      Type (4) Immediate Data
M0REXSSSSSSSSSDDDDDDDDDNNNNNNNNN      Type (5) General Operation
```

KEY

J - Reverse jump sense bit. Reverses logical sense of condition.

E - E bit. Reverses sign of carry input to ALU

X - An unused bit.

C - The condition code field.

T - The jump target field.

I - The immediate data field. Least significant seven bits are in first field, most significant nine bits in second field.

S - The nine bit source field.

D - The nine bit destination field.

N - The nine bit AM 2901 control field.

R - The return bit. Cause unconditional return combined with (4) or (5) type instruction.

M - The multiple precision bit. When on the ALU carry in is fed from the carry bit in the status register.

Arithmetic General Operation (Type 5) Instructions. The arithmetic operations are all General Operation (Type 5) instructions involving the Am 2901 arithmetic unit as the selected device in either the source field, destination field or both. Full control of the Am 2901 is only achieved when both the source and destination fields are devoted to selecting the Am 2901. In other cases enough bits are not available for full control. In practice this means that instructions involving shifts are not possible when the source or destination is external to the Am 2901. The source or destination select code for the Am 2901 is of the form: 10XXXXXXX. This means that only seven control bits are available if the Am 2901 is not both the source and destination. The 9-bit Am 2901 control field is partly appropriated to provide sufficient control when only one of the source and destination fields is available and this is the reason for the limited control.

The Am 2901 requires a 4-bit A field and a 4-bit B field to specify the source and destination address in the 16-word register file contained within the Am 2901. The nine bit, Am 2901, control field determines the arithmetic and logic unit (ALU) operation, destination of data and the type of shifting to be applied, if any. NOTE: An Am 2901 Data Sheet is attached as an Appendix.

EXAMPLE 1: Am 2901 Is The Source, Destination Other Device

Source Field:

8	7	6	5	4	3	2	1	0
1	0	B2	B1	B0	A3	A2	A1	A0

Am 2901 Control Field:

8	7	6	5	4	3	2	1	0
B3	I7	I6	I5	I4	I3	I2	I1	I0

The register field and B addresses for the Am 2901 are shown as A0-A3 and B0-B3. The Am 2901 control field bits are shown as I0-I8, to conform to the manufacturer's notation. In example 1 the bit normally assigned to I8 has been used to provide B3, since there are not enough bits in the source field. The Am 2901 unit sees a zero for bit I8.

EXAMPLE 2: Am 2901 is Destination, Source Is Other Device:

Destination Field:

8	7	6	5	4	3	2	1	0
1	0	A2	A1	A0	B3	B2	B1	B0

Am 2901 Control Field:

8	7	6	5	4	3	2	1	0
I8	I7	I6	I5	I4	I3	A3	I1	I0

In example 2 the A and B addresses are obtained from the destination field with the exception that A3 is obtained from the bit which would normally be control field bit I2. The Am 2901 sees a one for bit I2.

EXAMPLE 3: The Am 2901 Is Both Source and Destination:

Source Field:

8	7	6	5	4	3	2	1	0
1	0	ST	D1	D0	A3	A2	A1	A0

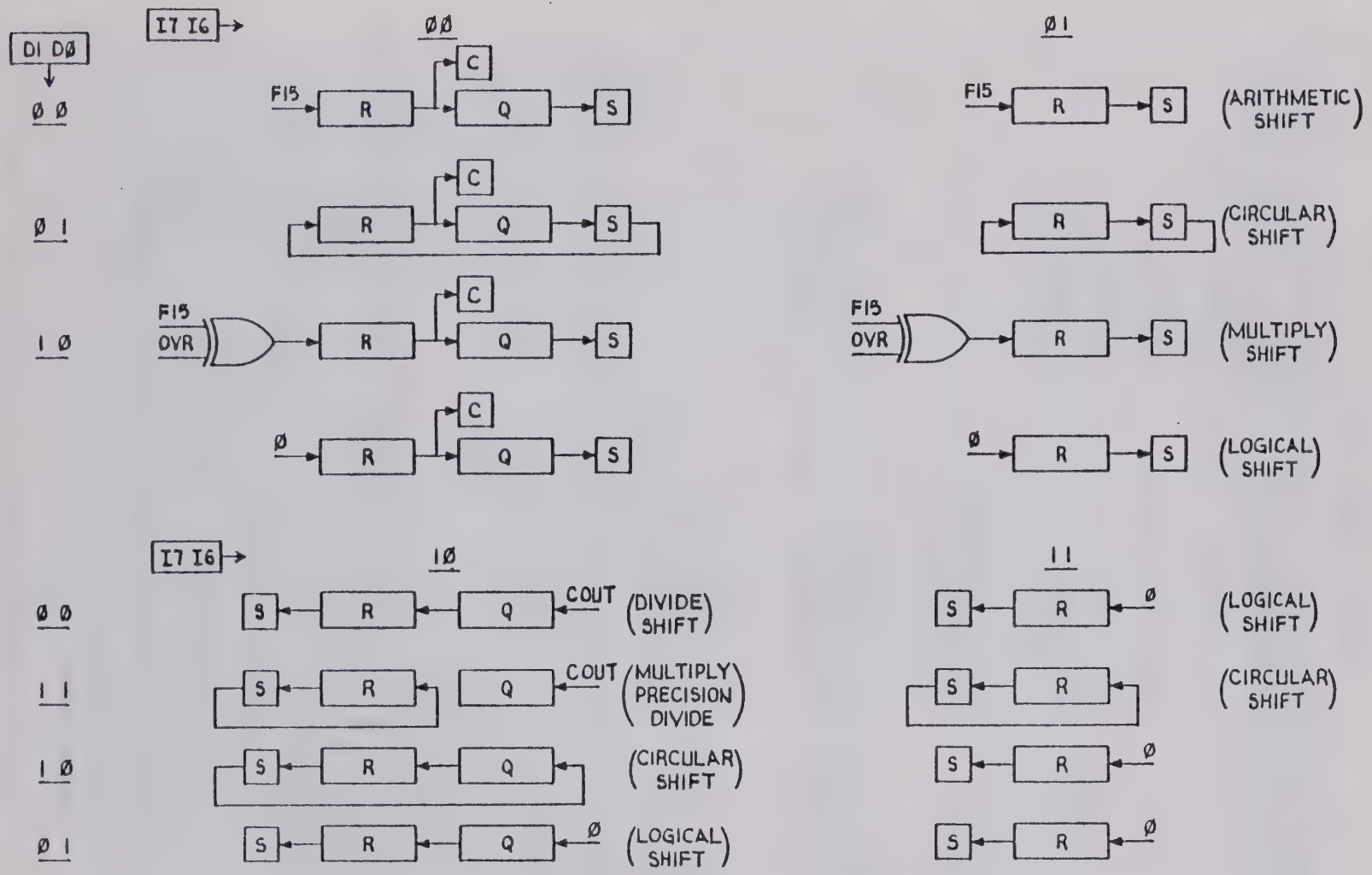
Am 2901 Control Field:

8	7	6	5	4	3	2	1	0
1	0	X	C1	C0	B3	B2	B1	B0

In example 3 both the source and destination fields are available. The Am 2901 control field is fed directly to the Am 2901, without using any bits to generate A and B addresses. The A and B addresses come directly from the least significant parts of the source and destination fields. The remaining bits in the source and destination fields are used to provide the following control bits:

- ST The store control bit,
- D1-D0 The shift control bits, and
- C1-C0 The ALU function modification bits.

The meaning of the shift control bits D1-D0 is shown in Table 3-1 and Figure 3-5. The store control bit, ST, must be a one for the result to be stored in the register file or the Q register of the Am 2901. The ST bit is only relevant for case 3 above. For case 1 and case 2, the storage or non-storage of the result depends upon the code in the Am 2901 control field. The control field code can also be used to inhibit storage of the result for case 3 above, but using this method of inhibiting the storage of the result is incompatible with shifts.



KEY

C	- STATUS REGISTER CARRY BIT
S	- STATUS REGISTER S BIT
R	- REGISTER FILE REGISTER
Q	- Am2901 Q REGISTER
FI5	- SIGN BIT OUTPUT OF Am2901 ALU
OVR	- OVERFLOW OUTPUT OF Am2901 ALU
COUT	- CARRY OUTPUT OF Am2901 ALU
I7-I6	- Am2901 CONTROL BITS I7, I6
DI-DØ	- SHIFT CONTROL BITS IN SOURCE FIELD

Figure 3-5. Am2901 Shift Modes

TABLE 3-1. Shift Control

CONTROL BITS I7	I6	D1	D0	SHIFT FUNCTION	
0	0	0	0	F15 →R-REG	→Q-REG →S →C
0	0	0	1	S → R-REG	→Q-REG →S →C
0	0	1	0	XF0 → R-REG	→Q-REG →S →C
0	0	1	1	0 → R-REG	→Q-REG →S →C
0	1	0	0	F15 → R-REG →S	
0	1	0	1	S → R-REG →S	
0	1	1	0	XFO → R-REG →S	
0	1	1	1	0 → R-REG →S	
1	0	0	0	S ← R-REG	←Q-REG ←COUT
1	0	0	1	S ← R-REG	←Q-REG ←0
1	0	1	0	S ← R-REG	←Q-REG ←S
1	0	1	1	S ← R-REG ←S	Q-REG ←COUT
1	1	0	0	S ← R-REG ←0	
1	1	0	1	S ← R-REG ←0	
1	1	1	0	S ← R-REG ←0	
1	1	1	1	S ← R-REG ←S	

Key to Shift Control

F15	Sign bit of ALU output.
S	Status register S bit.
C	Status register carry bit.
COUT	Carry out of ALU.
XFO	Exclusive or of ALU F15 and OVR outputs. This input repairs an overflow that happens during ALU operation.
I7, I6	Bits in Am 2901 control field.
D1, D0	Shift control bits.

NOTES

- S and C are flip-flops
- F15, COUT, XF0 are outputs from current ALU operation.
- The status register D bit is set by the COUT for certain C1, C0 control codes.
- The shifter is located between the ALU output and the registers.

The ALU function modification bits, C1-C0, cause certain modifications of the Am 2901 operation depending upon either the D bit of the status register (divide control) or the least significant bit of the Q register (multiply control). The effects of the possible C1-C0 codes are as follows:

00 - No modification to the Am 2901 control field.

01 - Control field bit I3 is inverted if the status register D bit is a one. The effect of inverting I3 is to change an addition to a subtraction, or vice-versa. The D bit provides divide control.

11 - I3 is inverted if the D bit is a one and at the end of the cycle the D bit is set to the value of the ALU carry out.

10 - Control bit I1 is inverted if the Q0 output is a one. The effect of inverting I1 is to change the ALU source input "A" from the register file to the constant zero, or vice versa. This is used to implement a multiply step, where either the multiplier, or zero, is added depending upon the least bit of the Q register.

The M and E bits influence the operation of the Am 2901 for examples 1, 2 and 3 above. For instructions not involving the Am 2901, the M and E bits are ignored. Together, the M and E bits control the carry input to the ALU. If both M and E are zero, the carry input is zero for an add operation and one for a subtract operation. This is the normal mode of operation. If the M bit is set to a one, the carry in is fed from the status register C bit. This allows multiple precision adds and subtracts. If the E bit is a one, the carry in is inverted, whatever its source. This allows increment and decrement operations. ALU operations which are not add or subtract are not influenced by the M or E bit settings.

Immediate Data (Type 4) Instructions. The immediate data instruction places 16 bits of data on the bus. This data is specified within the instruction word. The data is stored at the bus destination specified by the destination field in the instruction word. The least significant 7-bits of data come from bits 24-18 of the instruction word. The most significant 9-bits of data come from bits 8-0 of the instruction word. Specifying the Am 2901 as the destination of the immediate data is a special case, because the Am 2901 control field is taken up by the most significant part of the data. If the Am 2901 is selected as the destination the control field seen by the Am 2901 will have the code: 01D011111. The "D" means that the bit follows the data specified. However this uncontrolled bit does not influence the effective action of the Am 2901 which is to store the bus data in the register file location specified in the destination field as the B field. It is not possible to store immediate data directly in the Q register.

Unconditional Return (Immediate Data Type 4 and General Operation Type 5). If bit 29 of the instruction word is a one, for Immediate Data (Type 4) or General Operation (Type 5) instructions, an unconditional return is executed at the same time as the instruction. This means that the next instruction executed is not the next sequential instruction, but an instruction located at an address taken from the subroutine stack.

An unconditional return loads the instruction counter and the priority register from the subroutine stack. This results in a return to the instruction following a previous JSR (Type 2) or a return to the instruction following the last instruction executed before an interrupt. Usually a different priority is loaded only if the return is from an interrupt servicing routine, although it is possible that the interrupt priority had been explicitly changed in the subroutine and will be restored to the previous value as a result of the return.

Jump and JSR (Type 1 and 2) Instructions. If the condition test is passed as selected by the source/condition field, a jump to the target address is executed. The JUMP (Type 1) is a simple transfer of control. The JSR (Type 2) saves the return address and the current priority on the subroutine stack for a later return.

Conditional Return (Type 3) Instruction. The condition is tested as for Jump (Type 1) and JSR (Type 2) instructions. A return is executed if the condition is true, otherwise the execution continues with the next instruction.

Map Register ORing for Jump (Type 1), JSR (Type 2), Conditional Return (Type 3) Instructions. A 4-bit field can be stored with the target address for a Jump (Type 1) or JSR (type 2) instruction or with the return address for a conditional Return (Type 3) instruction. There are 4 choices of 4-bit Conditional Return fields, selected by special condition codes. A proper setting of the reverse jump sense bit assures that a jump or control transfer always takes place (otherwise the instruction would be a NOP). The effective destination address, where the next instruction is located, is the OR of the normal destination and the 4-bit field ORed into the least significant 4 bits. The four choices available are as follows:

- Map register lower nibble,
- Map register upper nibble,
- Status Register B-bit nibble,
- Code digit of the map register.

These choices are discussed more fully under the sections on the map register and status register.

The significance of the ORing is that a multiway jump (which is a function of data) can be accomplished. If the destination address has its least significant 4 bits zero it will be a 16-way jump. If one of the destination bits is a one, then the jump will be reduced to an 8-way jump, and so forth.

Interrupts and System Priority Level. The 3-bit priority register holds the current system priority level, from 0 to 7. An interrupt may have a hardware priority from 1 to 7. An interrupt will take place immediately if and only if the interrupt priority (determined by hardware) is higher than the system priority. If several interrupts are pending, the highest priority interrupt takes precedence. Precedence between interrupts of the same priority is determined by hardware interconnect, or in some cases by the interrupt routine. If the system priority is 7, no interrupts can take place, because there is no interrupt priority of level 8. If the system priority is 0, then all interrupts can take place.

When an interrupt takes place, the current instruction counter and priority level are stored on the subroutine stack. The instruction counter is loaded with an interrupt vector address, between 0 and 255, as determined by hardware wiring. The instruction located at the interrupt vector address is then executed. Usually it is a jump instruction pointing to the interrupt servicing routine.

Higher priority interrupts generally can interrupt servicing routines for lower priority interrupts. The exception would be if the interrupt servicing routine changes the interrupt priority level.

Conflicts Between Instructions and Interrupts. Change of control instructions generally conflict with interrupts, since both want to change the instruction counter, and in some cases the priority level and subroutine stack. In the case of a conflict with a Jump (Type 1), JSR (Type 2) or Unconditional Return (Type 3) instruction, the instruction is aborted by the hardware and the interrupt takes place. The address stored on the subroutine stack will be that of the aborted instruction, so that the aborted instruction will be read from control memeory a second time after the return from the interrupt and executed. In the case of a Immediate Data (Type 4) or General Operation (Type 5) instruction combined with an unconditional return, the instruction will be executed normally, but the associated unconditional return will not be executed. The unconditional return will be deferred until the return from the interrupt routine. The interrupt sequence in this case does not modify the subroutine stack, leaving it as is, since the return address is already on the top of the stack. These conflicts are usually not visible to the microprogrammer, but are explained here in order to aid understanding of the interrupt sequence.

Changing the Priority Level by Using Jump (Type 1), JSR (Type 2) or Unconditional Return (Type 3) Instructions. The priority register can be set to one of eight possible values by using one of eight different condition codes in a Jump (Type 1), JSR (Type 2) or Unconditional Return (Type 3) instruction. This method of setting the priority register is used because it avoids the conflict of an interrupt and an instruction both trying to set the priority register to different values at the same time. The conflict is avoided because Jump (Type 1), JSR (Type 2) or Unconditional Return (Type 3) instructions are aborted (to be executed later) if they conflict with an interrupt. The condition test will be controlled totally by the reverse jump sense bit. The priority will be set whether or not the condition test is passed.

Normally a Jump (Type 1) instruction is issued to set the priority. If a JSR (Type 2) is used, the priority stored on the subroutine stack will be the old priority (if the condition test is passed and the JSR (Type 2) instruction executes). This feature can be used to change the priority only for the duration of one subroutine. A Conditional Return (Type 3) instruction will only change the priority to the value specified in the condition code if the return does not execute. If it executes, the priority will come from the subroutine stack.

3.3.2.3 Microprocessor Registers. In the sections that follow the use and function of the various registers which may be accessed as sources and destinations on the bus are described. When mnemonics are used they are the mnemonics used by the Am 2901 microassembler.

Status Register. The status register is an 8-bit register which may be read and written as a data register attached to the bus, but in addition the various bits which make up the status register may be set and cleared independently by hardware to reflect the status of the microprocessor. When read or written as data the status register communicates with bits 8-15 of the data bus. The other 8 bits can be used, optionally, by the index register. The source and destination codes are as follows:

662 (SR) - If used in the source field the status register is output to the high byte of the bus. Zero is output to the low byte. If used as a destination, the high bus byte is stored in the status register, the low bus byte is ignored.

663 (XRSR) - May be used in either the source or destination fields. The status register communicates with the high bus byte, the index register with the low byte.

The 8-bits of the status register are defined as follows:

15	14	13	12	11	10	9	8
S	D	B	V2	N	X	V	C

Status Register Key Bit	Function
S -	The S bit is set by various shift instructions (see Figure 3-5).
D -	The D bit is set as a part of the divide algorithm. See the arithmetic General Operation (Type 5) Instructions for details.
B -	The B bit is set to zero when the low byte of the bus is stored in the map register. The B bit is set to one when the high byte of the bus is stored in the map register. The function of the B bit is to aid in constructing a stream of bytes from a stream of words.

V - The V bit is set or reset when the Am 2901 performs an add or subtract operation. If the result is wrong because of an overflow the V bit is set to one, otherwise zero. Non-Am 2901 operations, or non-add or subtract operations do not affect the value of the V bit.

V2 - The V2 bit is set under the same conditions as the V bit, but it is reset from a one to a zero only by storing data in the status register. It is an overflow bit that "sticks" on. The purpose is to check a chain of calculations for overflow, without having to waste the execution time for a test after every operation.

N - The N bit signifies a negative output from the Am 2901 ALU. It is set on, or off on any operation where the Am 2901 is a source or destination. In other operations its value is not affected.

Z - The Z bit indicates a zero output from the Am 2901 ALU. It is set or reset under the same conditions as the N bit. For both the N and Z bit the output of the ALU is tested before any shift of the data.

C - The C bit is set with the carry out of the Am 2901 ALU on an add or subtract operation except on the double right shift operation where it is set to the value of the bit shifted out of the register file part of the double right shift. If an operation is both add or subtract and double right shift, the double right shift controls the C bit. Operations other than those mentioned, or non-Am 2901 operations do not affect the value of the C bit.

In the case of a conflict in setting the status register, where a direct store from the bus is trying to set all bits and internal conditions are trying to set one or more bits, the direct store from the bus takes precedence.

Normally, the status register and the index register are saved on the data stack during interrupts. The combined mode of accessing the index register and the status register makes this faster.

Status Register Condition Codes. Condition codes exist so that conditional jumps may be made on each of the status register bits. In addition there exist condition codes for certain logical functions of the status register bits.

In the following table the 9-bit condition codes are given as octal numbers. A minus sign means that the reverse jump sense bit is a one; that is, the logical condition is reversed. The mnemonic names are those of the Am 2901 microassembler.

Table 3-2. Condition Codes

Mnemonic Code	Octal Numbers	Definition
LE	640	Less than or equal to zero. The Z bit is on, or else the N bit is on and the V bit is off or the N bit is off and the V bit is on.
QT	-640	Greater than zero. The logical reverse of LE.
LT	641	Less than zero. The N bit is on and the V bit is off or the N bit is off and the V bit is on.
GE	-641	Greater than or equal to zero. The logical reverse of LT.
CC	642	The carry bit is clear (zero).
CS	-642	The carry bit is set.
VC	-643	The overflow bit (V) is clear (zero).
VS	-643	The overflow bit is set.
NE	644	Not equal to zero. The Z bit is clear.
EQ	-644	Equal to zero. The Z bit is set.
PL	645	Plus. The N bit is clear.
MI	-645	Minus. The N bit is set.
V2C	646	V2 is clear.
V2S	-646	V2 is set.
BC	647	The B bit is clear.
BS	-647	The B bit is set.
DC	650	The D bit is clear.
DS	-650	The D bit is set.
SC	651	The S bit is clear.
SS	-651	The S bit is set.
NEV	652	Never true. Will not jump.
U	-652	Unconditional. Always jumps.
MRB	-654	If the B bit is on, the number 4 is ORed with the jump destination. If the B bit is off, zero is ORed with the destination, for no net change.

The Microprocessor Map Register. The map register is an 8-bit register which may be stored into from either the high or low byte of the data bus. The map register can supply either the high or low byte to the data bus while zeroing the other bus byte. Because of its ability to work from or to either bus byte the map register is useful for swapping bus bytes and performing shifts by 8 places on multiple precision numbers. In addition multiway jumps may be performed where either the upper or lower 4-bits of the map register are ORed in with the destination address. Always computed by hardware as a function of the current contents of the map register is the code digit, a 4-bit number which also may be used to control multiway jumps. The code digit functions are defined in the following table:

TABLE 3-3. Map Register Code

Map Register	Code Digit
76543210	3210
0xxxxxxx	0110 (6)
10xxxxxx	0111 (7)
110xxxxx	1000 (8)
1110xxxx	1001 (9)
11110xxx	1010 (10)
111110xx	1011 (11)
1111110x	1100 (12)
11111110	1101 (13)
11111111	1110 (14)

x - Indicates don't care bit.

As can be seen from the table above the code digit is related to the number of shifts needed to normalize a negative number stored in the map register.

The source and destination codes associated with the map register are as follows:

MRLO	666	Store the lower bus byte in the map register. (Destination)
MRHI	665	Store the upper bus byte in the map register. (Destination)
MRLO	665	Read the map register to the lower bus byte, zero to the upper bus byte. (Source)
MRHI	666	Read the map register to the upper bus byte, zero to the lower byte. (Source)

The following condition codes are associated with the map register:

MRC	-655	OR the code digit with the jump destination.
MRL	-656	OR the lower 4-bits of the map register with the jump destination.
MRU	-657	OR the upper 4-bits of the map register with the jump destination.

Scratchpad and Stack Memory. The scratchpad unit consists of a 256 word by 16-bit memory which may be addressed in several different ways with the aid of two 8-bit addressing registers, the index register and the stack pointer register. The stack pointer register is used to implement a last-in, first-out stack in a part of the 256 word memory. The index register can be used to address the memory by 16 word pages, or it can be used to implement a stack function. When either of the address registers are used to implement a stack, the register is incremented before any data is stored into memory and decremented after data is removed from memory. The memory address is always the sum of the contents of the address register and the last 4 bits of the source or destination code. The actual increment or decrement takes place at the end of the memory access cycle. The pre-increment is accomplished by temporarily adding one to the address during the cycle to simulate an increment at the beginning of the cycle.

The significant source and destination codes are as follows:

XR	661	As a destination store the lower 8 bits of the bus in the index register. As a source put the lower 8 bits on the bus and zeros in the upper 8 bus bits.
XRSR	663	Use as source or destination to transfer between the index register in the lower 8 bits and the bus.
XSTK	664	Use as a source or destination to communicate between the lower 8 bus bits and the stack pointer register. If a source, the upper 8 bus bits are set to zero.
STK	637	Use as source or destination to push or pop from the stack defined by the stack pointer register (XSTK). The top of the stack is located at the address pointed to by XSTK. The stack works by incrementing the stack pointer after data is read from the scratchpad. When data is written into the scratchpad the stack pointer is decremented before the write operation.
SP0,SP1-SP15	600,601-617	Use as a source or destination to address the 16 locations of the scratchpad starting at the location pointed to by the index register.

XST0,XST1-XST14	620, 621-636	Address the location pointed to by the index register with 0 to 14 added and a pre-increment if a source or a post-decrement if a destination. Can be used to establish a stack or to move successive words in or out of memory in a loop. Note that this stack function is different from STK, in that the pointer register (XR) is post decremented for a write and pre-incremented for a read.

It is impossible for the scratchpad to be both a source and destination in the same instruction. The scratchpad memory and either of the addressing registers are permitted to both be addressed in the same instruction. No confusion will result from this if it is remembered that the pre-increment is only simulated and that a load to the addressing register suppresses any counting.

3.3.3 PROM Board Circuit Descriptions

The following text is primarily referenced to the diagrams listed below:

Block Diagram	Figure 3-6
Detailed Schematic	2501-4701-2D

The PROM board contains the microinstruction program memory and the stack-scratchpad memory discussed in the paragraph on the Processor, and several miscellaneous functions including Real Time Clock, Interrupt Interface, Fractional Multiplier, and Thermal Printer Interface. These circuits are described individually in the following paragraphs.

3.3.3.1 Program Instruction Memory. This memory contains instructions which are read out and executed by the 2501 microprocessor. Input is 16 address lines from the instruction counter which enter at the card edge (IC0-15). The least significant 10 bits are buffered and inverted by U40 and U42. Buffered address lines RA0-9 are fed directly to the PROM chips. The most significant bits of the address lines are decoded to provide chip select signals to various banks of PROMs (see Figure 3-7). Output is 32 PROM data lines, labeled ROMDAT0-8, D0-8, S0-8 and ROMDAT 27-31. These lines are fed off the card at the card edge (E1L, E2L, E1M, E2M, E1N).

Three types of PROMs may be used: 512x8 (Intel 3624), 1024x8 (Intel 3628), 2048x8 (Signetics 82S191). Other PROM types, with the same pin configurations may be used provided they have a 75 ns worst case access time and 3-state outputs. Different size PROMs may be installed in different banks provided holes in the address space are taken into account during programming. There are 6 banks of PROMs, U16-39, on the 2501-4701 board. Each bank provides 512, 1024 or 2048 instructions of 32 bits (see Table 3-4). As manufactured, the card has PC traces to jumper the card for 1024x8 PROMs. These traces must be cut before jumpers or different size PROMS may be installed.

NOTE

The PROM may be disabled by pulling -EXPROMDISAB low at Pin F2V. This allows for use of writable control store.

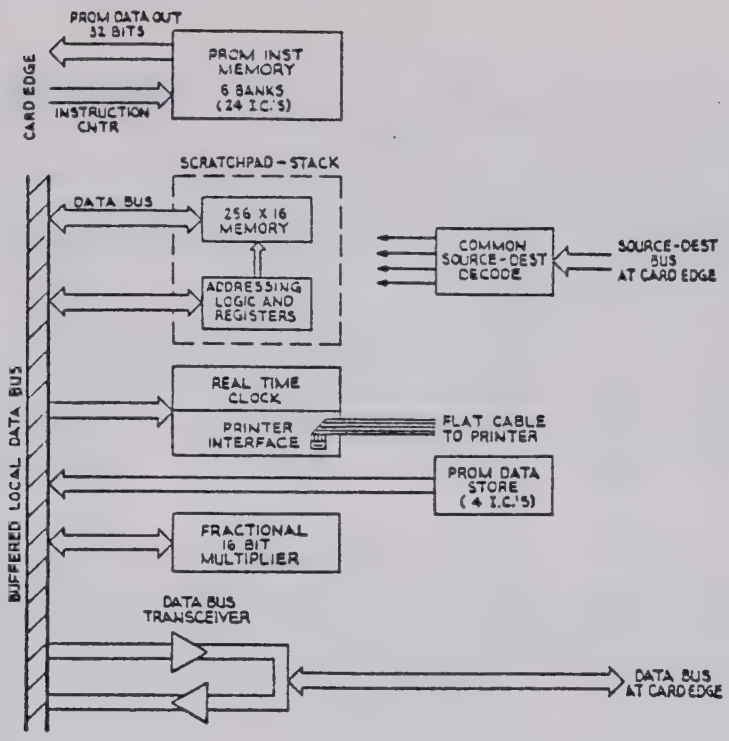


Figure 3-6. PROM Board Block Diagram

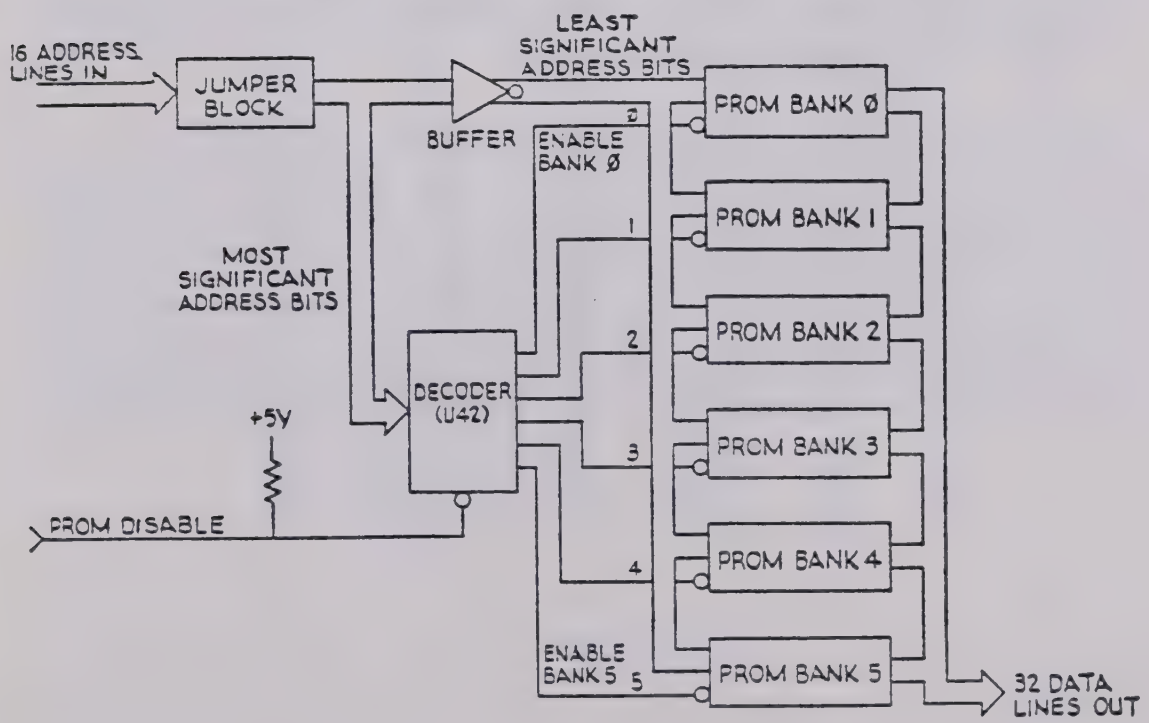


Figure 3-7. Instruction Memory Block Diagram

TABLE 3-4. RELATION OF PROMS TO OUTPUT DATA

	OUTPUT BITS				BANK OCTAL ADDRESSES BY PROM TYPE		
	Bits 0-7	Bits 8-15	Bits 16-23	Bits 24-31	512x8	1024x8	2048x8
Bank 0	U32	U20	U38	U26	0-777	0-1777	0-3777
Bank 1	U31	U19	U37	U25	1000-1777	2000-3777	4000-7777
Bank 2	U30	U18	U36	U24	2000-2777	4000-5777	10000-13777
Bank 3	U29	U17	U35	U23	3000-3777	6000-7777	14000-17777
Bank 4	U28	U16	U34	U22	4000-4777	10000-11777	20000-23777
Bank 5	U33	U21	U39	U27	5000-5777	12000-13777	24000-27777

OUTPUT BIT - SIGNAL NAMES - EDGE CONNECTOR

Bit	Signal	Pin	Bit	Signal	Pin
0	ROMDAT0	E2E	16	D7	D1L
1	ROMDAT1	E1F	17	D8	D2L
2	ROMDAT2	E2F	18	S1	D1B
3	ROMDAT3	E1H	19	S1	D1B
4	ROMDAT4	E2H	20	S2	D2B
5	ROMDAT5	E1S	21	S3	D1C
6	ROMDAT6	E2S	22	S4	D1D
7	ROMDAT7	E1K	23	S5	D2D
8	ROMDAT8	E2K	24	S6	D1E
9	D0	D2F	25	S7	D2E
10	D1	D1H	26	S8	D1F
11	D2	D2H	27	ROMDAT27	E1L
12	D3	D1J	28	ROMDAT28	E2L
13	D4	D2J	29	ROMDAT29	E1M
14	D5	D1K	30	ROMDAT30	E2M
15	D6	D2K	31	ROMDAT31	E1N

3.3.3.2 Stack Scratchpad Memory. This unit is built around a 256 x 16 bit fast bipolar memory. The memory can be written from or to the microprocessor data bus in various ways. The index register (XR) and the stack pointer register (XSTK) are each 8-bit up-down counters used to generate and hold the 8-bit addresses used to address memory (see Figure 3-8). All addresses are generated modulo 256. Address 0 follows address 255. There are two modes of addressing available using the index register (XR). In one mode the index register is set to an address which represents the base of a 16 word page. Any of 16 words can then be written or read with 16 source and destination codes without resetting the index register. In the other mode of addressing (the index register) a 15 word page is accessible and the index register is incremented before a word is read or after a word is written, thus shifting the whole page up or down. This pre-increment, post decrement mode of addressing may be used to read succesive words in a loop or to implement a stack using the index register.

The stack pointer register (XSTR) has only one mode of addressing. A store with destination code 637 does a push to the stack. A read with source code 637 does a pop from the stack. The stack pointer is incremented for a pop and decremented for a push (see Figure 3-9). The stack grows toward lower addresses. In the software documentation the pop is described as a post increment, that is, the stack pointer is incremented after the data is read, and the push is described as a pre-decrement. This is the easiest way to understand and utilize what is happening from the software standpoint. However from the hardware point of view it is actually a pre-increment and a post-increment. All actual incrementing and decrementing of the counters is always done at the end of the read or write cycle on the master clock. But when a pre-increment is desired a one is added to the address with an adder during the cycle so that the effective address is incremented at the start of the cycle, although the counter only counts up at the end of the cycle.

When the index register is used to address memory, the memory address is formed by adding together the contents of the index register and the least 4 bits of the source or destination code, a constant of 16 and 1 if it is a source mode involving a pre-increment. The constant 16 is added only if the index register is selected by feeding a bit into bit 4 of the adder. When the stack pointer is used the address is formed by adding together the contents of the stack pointer register, the least 4 bits of the source or destination code which is always 15 and a 1 if the operation is a pop. What the programmer thinks are addresses 0-255 in the memory are actually 16 to 15, passing through 255, 0, 1, etc. The physical addresses in the memory are unimportant since the programmer only can use the two index registers to address the memory.

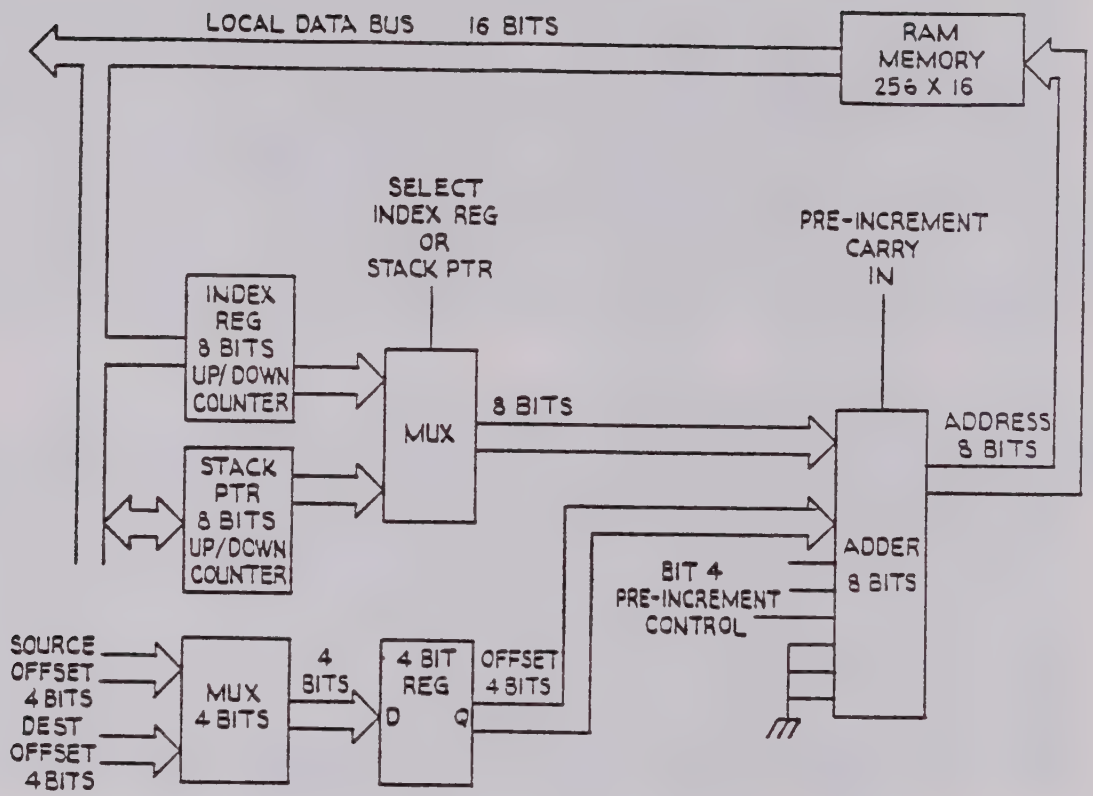


Figure 3-8. Scratchpad Stack Block Diagram

TABLE 3-5. SOURCE & DESTINATION CODES

Source/ Destination Code			4SELS	Count Stack PTR	Count Index Reg	Addressed Source	Location DEST	Mnemonic
6	0	0	0	0	0	XR+16	+0	SP0
6	0	1	0	0	0	XR+16	+1	SP1
6	0	2	0	0	0	XR+16	+2	SP2
6	0	3	0	0	0	XR+16	+3	SP3
6	0	4	0	0	0	XR+16	+4	SP4
6	0	5	0	0	0	XR+16	+5	SP5
6	0	6	0	0	0	XR+16	+6	SP6
6	0	7	0	0	0	XR+16	+7	SP7
6	1	0	0	0	0	XR+16	+8	SP8
6	1	1	0	0	0	XR+16	+9	SP9
6	1	2	0	0	0	XR+16	+10	SP10
6	1	3	0	0	0	XR+16	+11	SP11
6	1	4	0	0	0	XR+16	+12	SP12
6	1	5	0	0	0	XR+16	+13	SP13
6	1	6	0	0	0	XR+16	+14	SP14
6	1	7	0	0	0	XR+16	+15	SP15
6	2	0	0	0	1	XR+16+1	XR+16+0	XST0
6	2	1	0	0	1	XR+16+2	XR+16+1	XST1
6	2	2	0	0	1	XR+16+3	XR+16+2	XST2
6	2	3	0	0	1	XR+16+4	XR+16+3	XST3
6	2	4	0	0	1	XR+16+5	XR+16+4	XST4
6	2	5	0	0	1	XR+16+6	XR+16+5	XST5
6	2	6	0	0	1	XR+16+7	XR+16+6	XST6
6	2	7	0	0	1	XR+16+8	XR+16+7	XST7
6	3	0	0	0	1	XR+16+9	XR+16+8	XST8
6	3	1	0	0	1	XR+16+10	XR+16+9	XST9
6	3	2	0	0	1	XR+16+11	XR+16+10	XST10
6	3	3	0	0	1	XR+16+12	XR+16+11	XST11
6	3	4	0	0	1	XR+16+13	XR+16+12	XST12
6	3	5	0	0	1	XR+16+14	XR+16+13	XST13
6	3	6	0	0	1	XR+16+15	XR+16+14	XST14
6	3	7	1	1	0	XS+16	XS+15	STK

Additional Source & Destination Codes Associated

S661, S663 — read under register to lower 8 bits of bus

D662, D663 — Store lower 8 bits of bus to under register

S664 — Stack pointer to lower 8 bus bits

D664 — Lower 8 bus bits to stack pointer

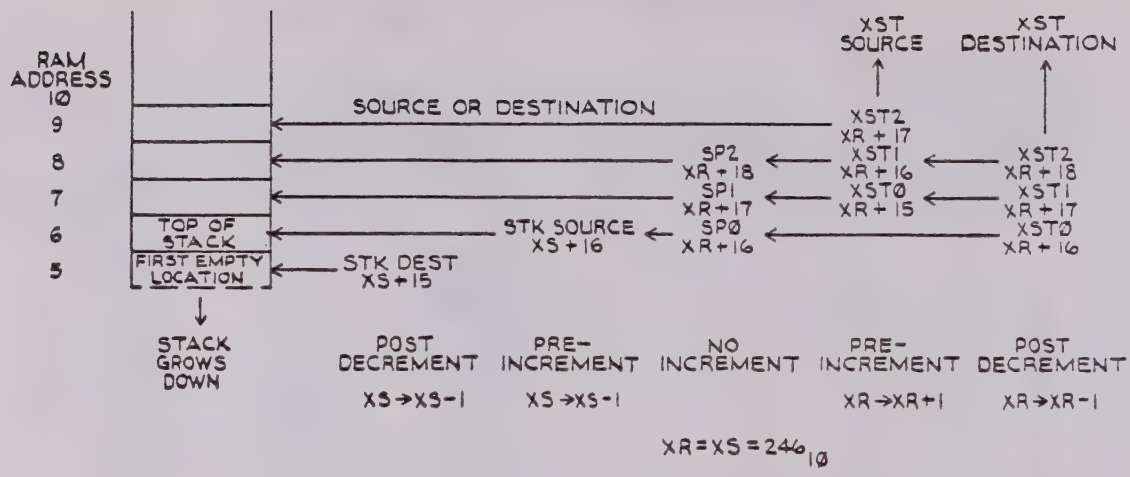


Figure 3-9. Example of Scratchpad Addressing Modes

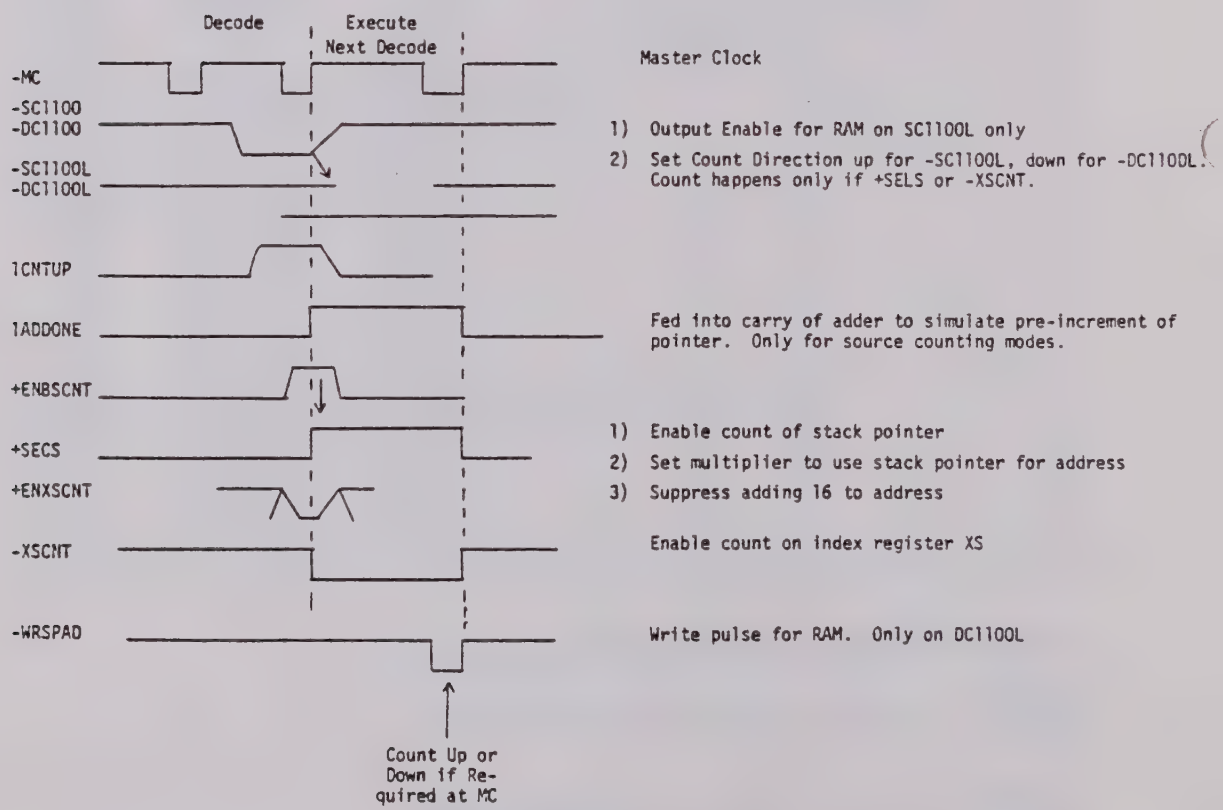

Decode
Execute
Next Decode
-MC
Master Clock
-SC1100
-DC1100
1) Output Enable for RAM on SC1100L only
2) Set Count Direction up for -SC1100L, down for -DC1100L. Count happens only if +SELS or -XSCNT.
-SC1100L
-DC1100L
1CNTUP
1ADDONE
Fed into carry of adder to simulate pre-increment of pointer. Only for source counting modes.
+ENBSCNT
+SECS
1) Enable count of stack pointer
2) Set multiplier to use stack pointer for address
+ENXSCNT
3) Suppress adding 16 to address
-XSCNT
Enable count on index register XS
-WRSPAD
Write pulse for RAM. Only on DC1100L
Count Up or Down if Required at MC

Figure 3-10. Stack-Scratchpad Generalized Timing Chart

3.3.3.3 Real Time Clock. The real time clock is a 16 bit counter which counts every 4 μs. The 4 μs period signal which drives the 16 bit counter is derived from the 16 MHz master clock available on the backplane (see Figure 3-11). Actual counting happens at the master clock, rather than exactly at the 4 μs clock. The first master clock after the 4 μs clock makes a transition is used to count the Real Time Clock. Thus there is some jitter in the time at which the clock counts (never more than 1 μs) but there is no cumulative error. The clock counter is a ripple counter which takes about 250 ns to count due to the time for the carry to ripple from one end to the other (see Figure 3-12). Because the real clock counts synchronously with the master clock it can be read directly onto the data bus (through a buffer) without fear that it will be changing its value as it is being read. However it does take 250 ns to settle down after the master clock. Therefore it is necessary to stretch any instruction involving the clock as a source so that the clock will be stable by the time the data is clocked into the destination. When the clock is supplied to the bus, a delay of 6 clocks (375 ns) is enabled. The clock is never cleared or reset except when the microprocessor is initialized. In that case it is cleared to zeros. The period of the clock is 262.144 ms with the 16 MHz clock on the backplane.

Associated with the realtime clock is a 16-bit clock compare register (U105 + U106) and a 16 bit equal-not equal comparator (U107 and U108). The clock compare register may be loaded from the microprocessor bus. Just before the clock is counted the contents of the clock are compared with the contents of the clock compare register. If they are equal, a +EQUAL signal is generated. The +EQUAL signal may cause an interrupt of the microprocessor or cause action in the printer interface. Both the count and the compare happen at the rising edge of the +CNTRU signal. An equal compare signal is captured by flip-flop (U116) at this time.

The final register associated with the realtime clock is the 8-bit clock hold register. The object of the clock hold register is to overcome the effects of interrupt latency so that the firmware can tell the exact time at which an interrupt signal (I0) was requested. The clock hold register captures the least 8 bits of the clock when interrupt flip-flop (U113) I0 is enabled (part of interrupt-printer interface). The data is captured synchronously with the master clock. Since only the least 8-bits are captured the interrupt latency must be less than 255 clock counts, or 1 millisecond, for the firmware to be able to reconstruct the time at which the clock hold register was clocked.

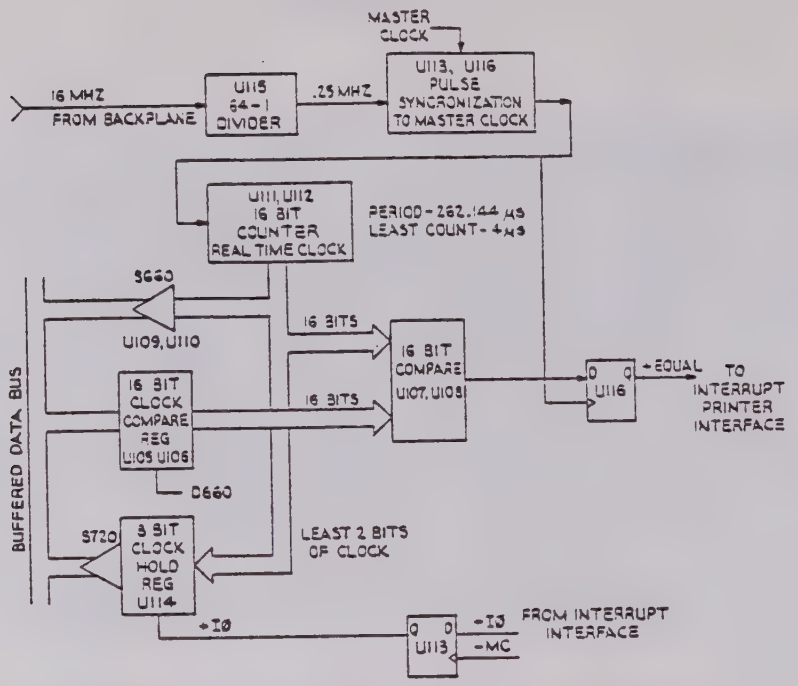


Figure 3-11. Real Time Clock Block Diagram

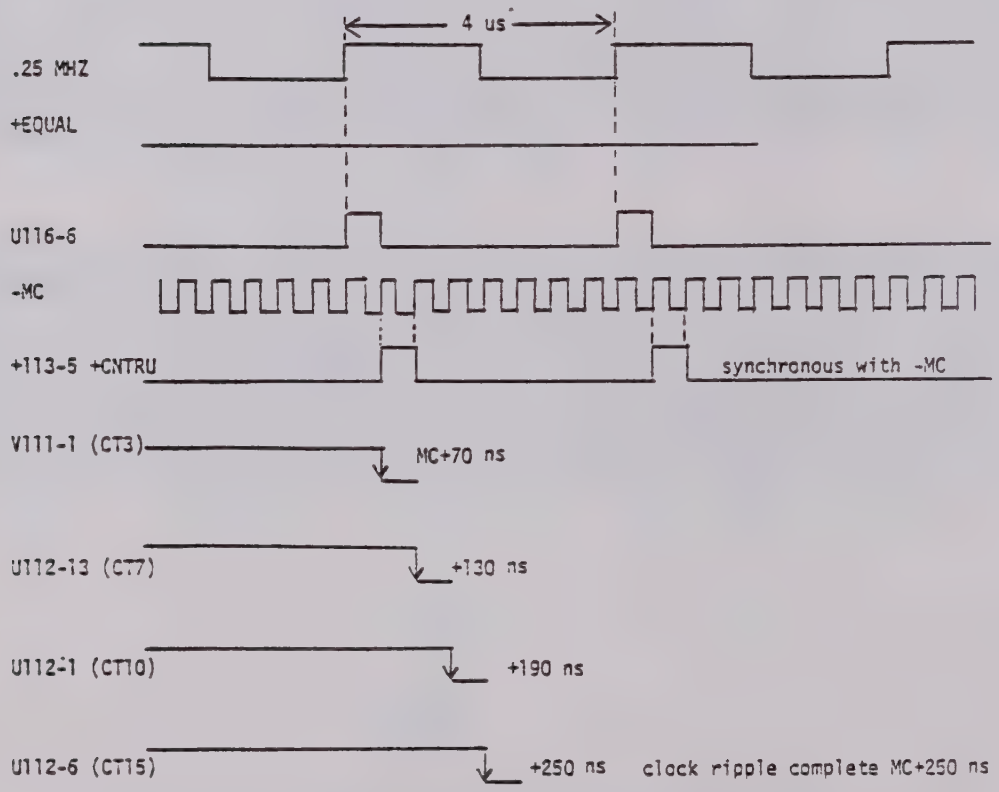


Figure 3-12. Syncronization of Real Time Clock with Master Clock

3.3.3.4 Interrupt Interface. There are 4 interrupt flip-flops in the interrupt interface, designated I0 - I3 (see Figure 3-13). If any of these flip-flops are set active a 2501 microprocessor interrupt is requested (204 base 8, priority 6). The flip-flops are not reset by the interrupt but must be reset by the firmware which can read the state of each and reset each. To prevent multiple interrupts it is the responsibility of the firmware to reset all the flip-flops before lowering the interrupt priority in the interrupt servicing routine. The microprocessor firmware has the option of disabling any or all of the interrupt flip-flops by leaving the reset bits at zero, thus holding the flip-flop corresponding to the reset bit in a reset condition. The flip-flops are set by negative to positive transition on the clock input. The clock inputs to the various flip-flops are as follows:

I3 Set when an equal compare condition is detected in the real time clock. Principal function of I3 is to turn off the printer heaters at the end of a burn but may also be used to generate an interrupt at a time held in the clock compare register.

I2 Set when the real time clock overflows. That is when the count changes 65536 to 0. Purpose is to allow firmware to extend the clock to multiple word length.

I1 Set by a transition on input pad T2. The sense of the transition recognized can be inverted by changing control bit SN1. An interrupt can also be caused by cycling SN1 through a transition, holding the input pad T2 constant (e.g., nothing connected to T2). The major function of I1 is to create an artifical interrupt by cycling SN1 to call the task arbitrator.

I0 The clock input to I0 is from a 1 of 8 selector. In addition, the polarity of the input can be reversed by control bit SN0. Thus I0 is multifunctional. The functions which can be selected are:

- Print zone on T80 printer,
- Dot row strobe on T80 printer,
- Character strobe on T80 printer,
- DECIN or pad T2, the same signal as I1 uses,
- Paperfeed button on case of T80 printer pressed,
- Input pad T4,
- Input pad T5,
- Equal compare, the same signal as used by I3.

The main functions of I0 are to turn on the printer heaters at the dot row strobe and to cause an interrupt if the operator pushes the paperfeed button. Which of the 8 inputs is selected is controlled by the binary value in the 3 control bits (SEL0, 1, 2). These may be set by the firmware. The clock input to I0 is filtered so that pulses shorter than about 200 ns are ignored. This is to prevent noise on long printer cables from causing false triggers.

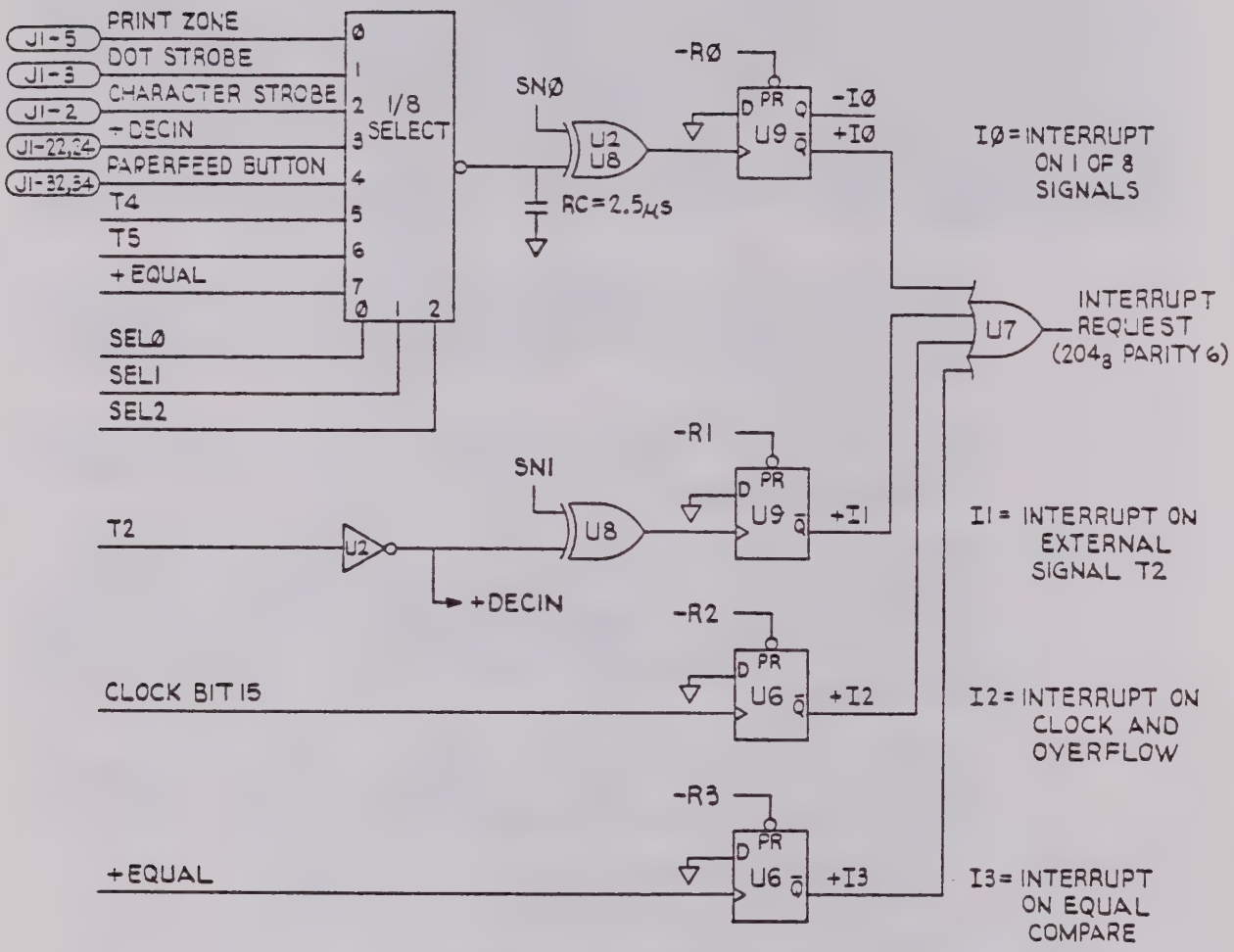


Figure 3-13. Interrupt Interface Block Diagram

3.3.3.5 T80 Printer and Interface. A print head with 7 resistive heaters moves across the page at a uniform rate of speed. The resistive heaters are pulsed on for periods between .5 and 1.5 ms to make dots on the paper, which is sensitive to heat. When the print head reaches the extreme right edge of the paper or the end of the printing, a carriage return starts, the print head moving back at a faster rate. Printing one line takes 1 second. While the carriage return takes place the print head is lifted and line feeds are started. Each line feed moves the paper 1/60th of an inch and either 6 or 10 line feeds are required, depending upon the mode of printing (see Figure 3-14). Unless the print line is short the line feeds are completed by the time the print head returns to the home position.

The print head heaters are turned on and off by the firmware program. Synchronizing pulses are sent from a slotted disk-photocell arrangement in the printer. There is one line which provides a pulse for each row of dots. Another line provides a pulse every 7 dot rows, or at each character position. A third photocell device sends a signal which goes high when the print head enters the print zone, approximately an inch from the left side of the paper. Once the head has reached the print zone printing can start. Conversely once the head leaves the print zone on a carriage return, the next line can be started.

The print head heaters in the T80 printer can damage the platen if left on for a prolonged period. Some effort has been taken to avoid this possibility by a failsafe design (see Figure 3-15). Unplugging the interface cable, or unplugging any cable in the 2501 microprocessor will turn the heaters off. A programming error in the firmware program will not burn the platen unless the program was deliberately written to burn the platen. Pullup resistors at both the interface on the PROM board and on the printer disable the heaters if the cable is disconnected. The heaters are active low in the cable. If the software fails to turn off the heater for any reason, a hardware watchdog timer turns them off automatically in about 25 ms. Each time the heater interface register is loaded, the watchdog timer is reset and starts counting. If it reaches 25 ms, the enable on the 3-state driver is deactivated allowing the pullup resistors to turn off the heaters. Since normal heater burn time is a few milliseconds, the watchdog timer has no effect unless the heaters are left on longer than the normal burn time. The watchdog timer is a counter driven by a local RC oscillator. A local oscillator is used because timing signals from the backplane could be lost if other boards are unplugged.

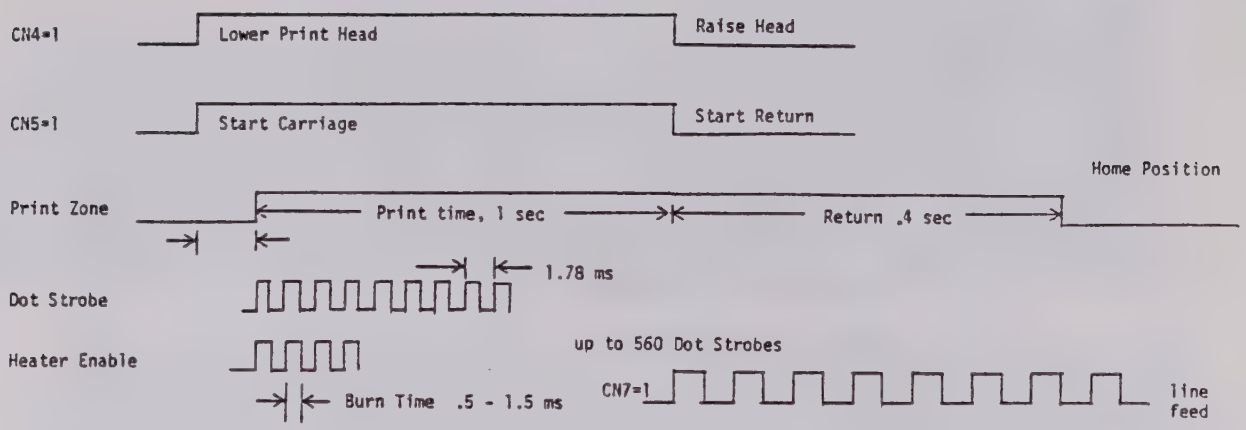


FIGURE 3-14. T80 Printer Operation Timing Chart

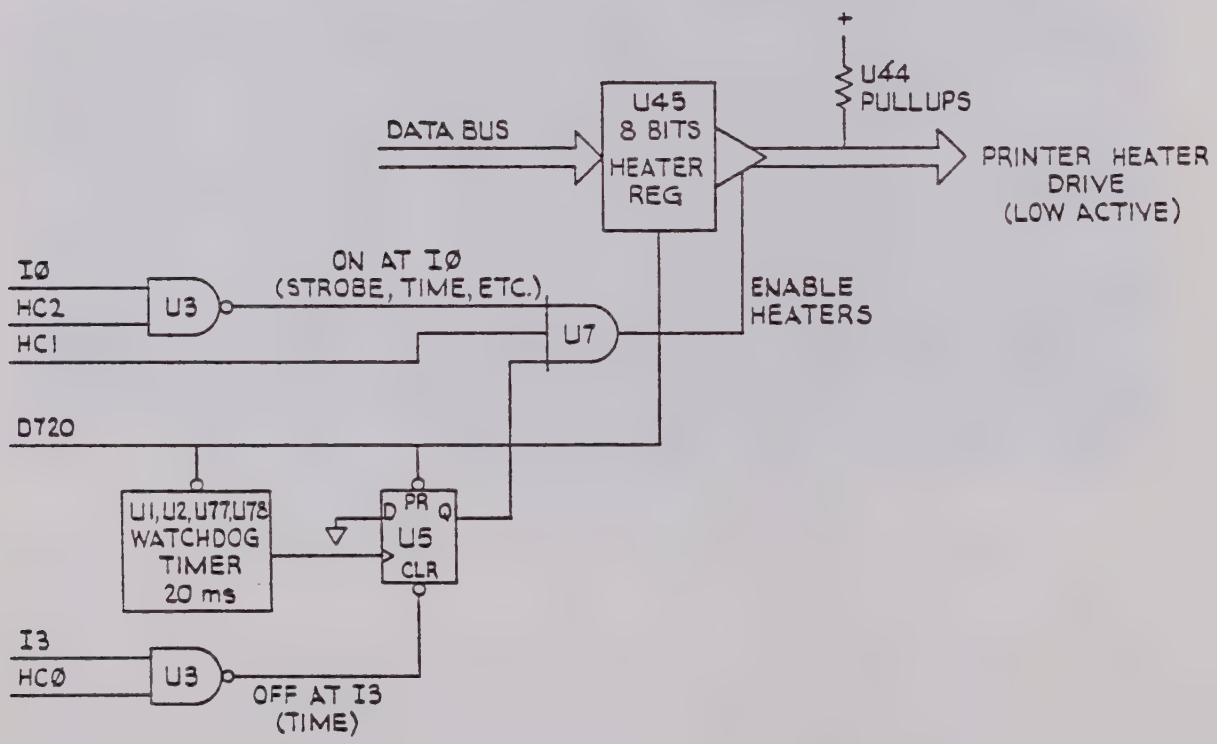


Figure 3-15. Printer Heater Enable Circuit

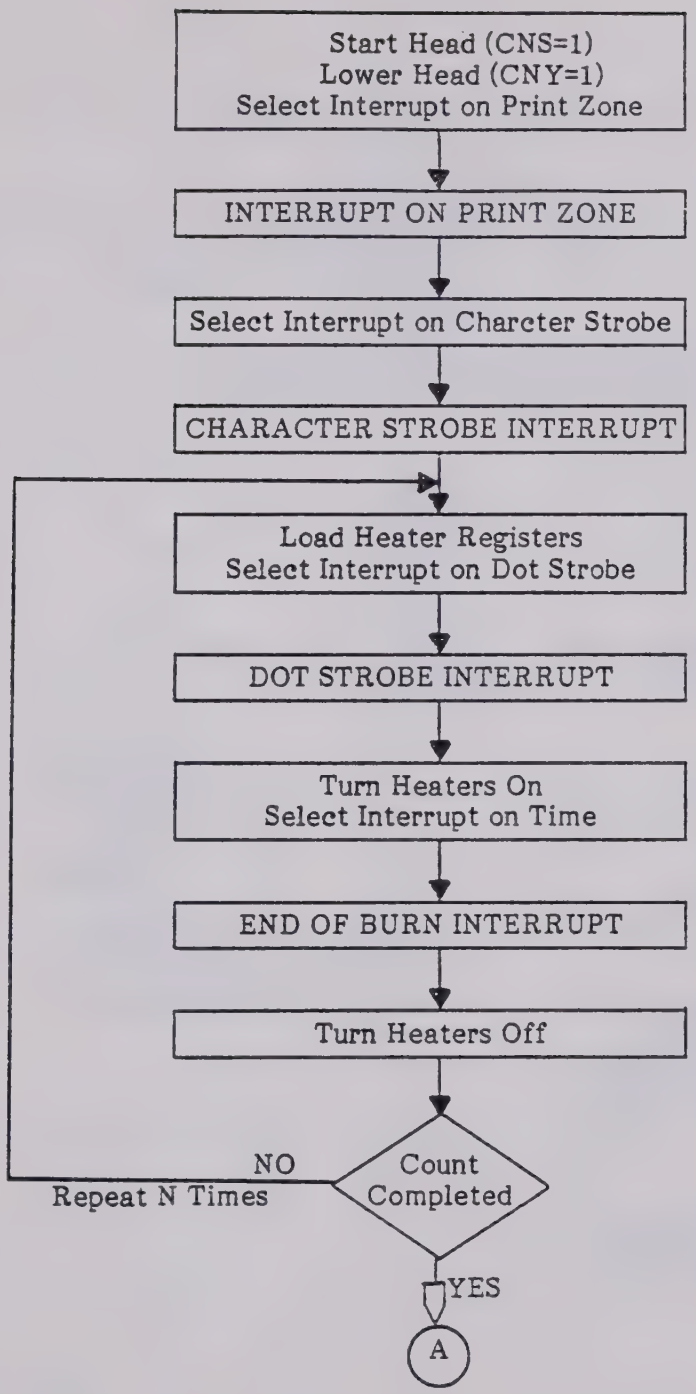


Figure 3-16. Typical Printer Operating Sequence

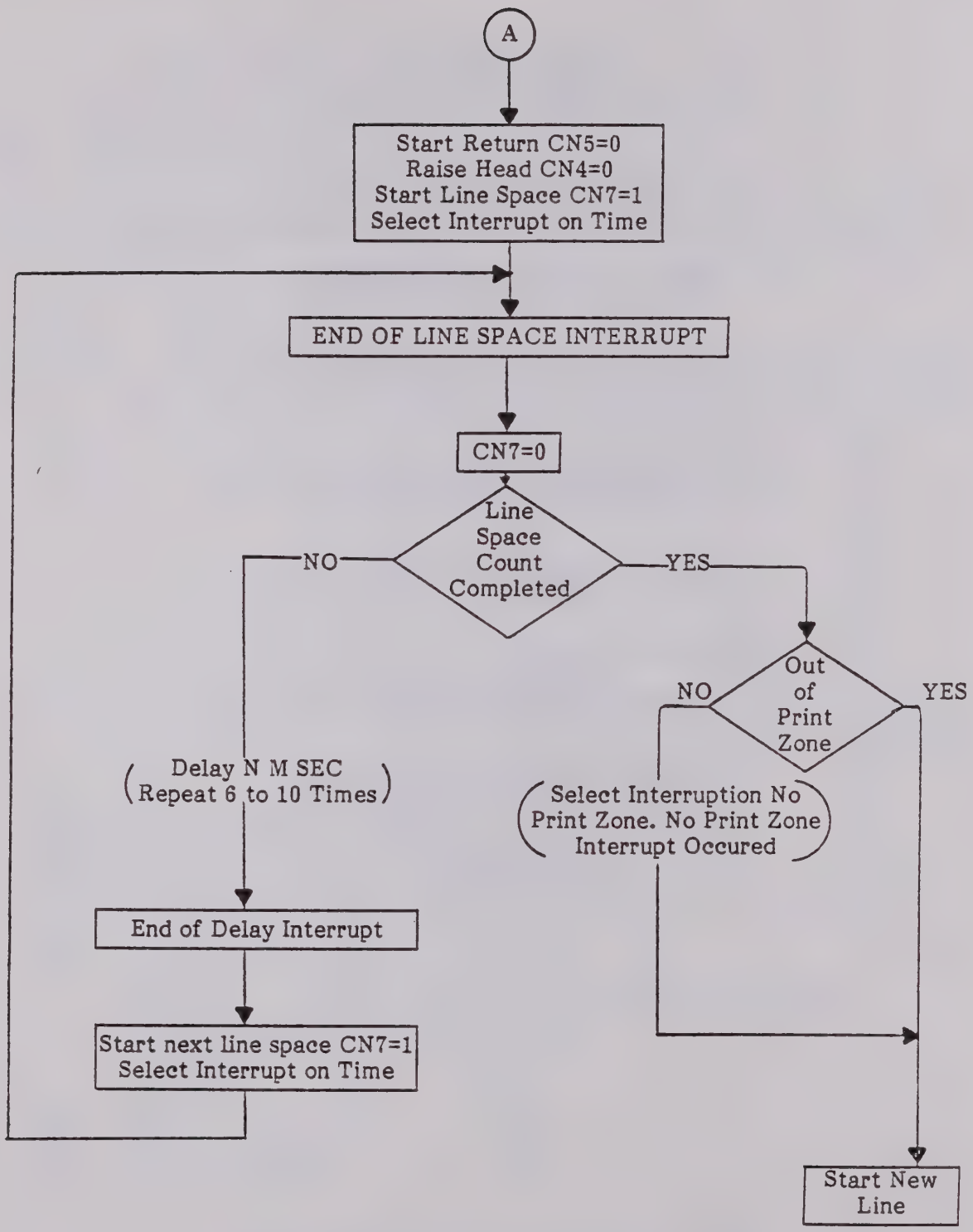


Figure 3-16. Typical Printer Operating Sequence (Continued)

TABLE 3-6. T80 Printer Control Lines

Control Bit	T80 Signal Name	Connector Number PROM Board	Effect of Control Bit
CN5	-AVIN0	J1-11	1 - Start Head Moving Right 0 - Home Head, Start Return
CN4	-SALON	J1-9	1 - Lower Head to Paper 0 - Raise Head
CN7	UM02	J1-6	1 - Begin Line Feed 0 - End Line Feed, No Line Feed
H0	-SCA00	J1-19	
H1	-SCA01	J1-20	
H2	-SCA02	J1-21	0 - Enable Heater
H3	-SCA03	J1-22	1 - Disable Heater
H4	-SCA04	J1-23	
H5	-SCA05	J1-24	
H6	-SCA06	J1-25	
H7	-ICA0		
CN0	Not Used	J1-33 (F2N F1N)	0 - Transition beeps beeper in keyboard (Located in GenRad keyboard, not in T-80)

TABLE 3-7. T80 Sense Lines

Description Line	Sense Bit	T80 Signal Name	T80 Connector	Meaning of Line
Print Zone*		+SLIN0	J1-5	Positive when head is in print zone
Dot Strobe*		+SPUNO	J1-3	Positive pulse at each dot position
Character Strobe*		+SCRTO	J1-2	Positive pulse at character position (every 7 dots)
Paperfeed Button*	CI5		J1-32	Signal and bit remain negative while paper feed button held down
Print Intensity Thumbwheel	CI4 CI5 CI6 CI7	TEM0N TEM1N TEM2N TEM3N	J1-28 J1-30 J1-14 J1-31	4 bit print intensity code with values 0-9. Values 10-15 may happen while thumbwheel in motion.
Alarm/Clear	CI8		J1-15	Signal and bit remain negative while Alarm/Clear button on T80 case depressed.
Print Unit Connected	CI3		J1-29	1 - Printer not connected 0 - Printer connected
Manual Head Lift	CI0	-ALBAA	J1-4	0 - Head up by manual lever in case 1 - Head free
Manual Line Feed	CI1	ITMA0	J1-12	0 - Manual line feed not activated 1 - Manual line feed inside case activated.

*Signal that may cause an interrupt I0

TABLE 3-8. Heater Enable Control Bits

Control Bits		Functions
HC1	0 -	Unconditional disable
	1 -	Conditional enable depending HC2, HC0
HC2	0 -	Disable on-at-I0 feature
	1 -	Enable on-at-I0 feature (force on)
HC0	0 -	Disable off-at-I3 feature (force on)
	1 -	Enable off-at-I3 feature

BASIC FUNCTIONAL COMBINATIONS OF HEATER CONTROL BITS

HC0	HC1	HC2	
0	X	X	Disable heaters
1	1	0	Enable if I0 on
1	0	1	Enable unless I3 on
1	1	1	Enable if I0 and not I3
1	0	0	Enable heaters unconditionally
I0	Happens at		Dot strobe Character strobe Equal compare (time)
I3	Happens at		Equal compare (time)

3.3.3.6 Fractional Multiplier. The fractional multiplier uses 2 AMD chips (U96 and U95) to do the multiply. A 16 bit shift register (U93 and U94) holds one of the multipliers and the result. To perform a multiply the first number is loaded in the shift register (U94 and U95) D722. (See Figure 3-17.) This clears the 4-bit cycle counter (U98). The second number is loaded into the multiplier at D723. Loading the second number starts the multiply which requires 33 clocks of the 16 MHz clock. The first clock loads the least significant bit from the shift register to the sign extend flip-flop (U100) and loads a one bit into the multiplier so that the result will be rounded. The following 32 clocks perform the multiply. After the sign bit enters the sign extend register, the contents of the sign extend register are frozen for the remaining clocks, to extend the sign as shown in figure 3-18. The result is read from shift register via S722. The result is scaled so that 32768=1.0, 16384=.5, etc. If 16384 x16384 are multiplied the result will be 8192. Positive and negative numbers are acceptable and the sign will follow the rules of arithmetic. The multiplication -32768x-32768 will result in -32768 which is incorrect and an overflow condition due to the fact that +32768 cannot be represented in 16-bits in 2's complement notation. Rounding always takes place and is effected by adding +1/2 to the least significant bit. A test at condition code 723 indicates if the multiplier has completed the multiplication.

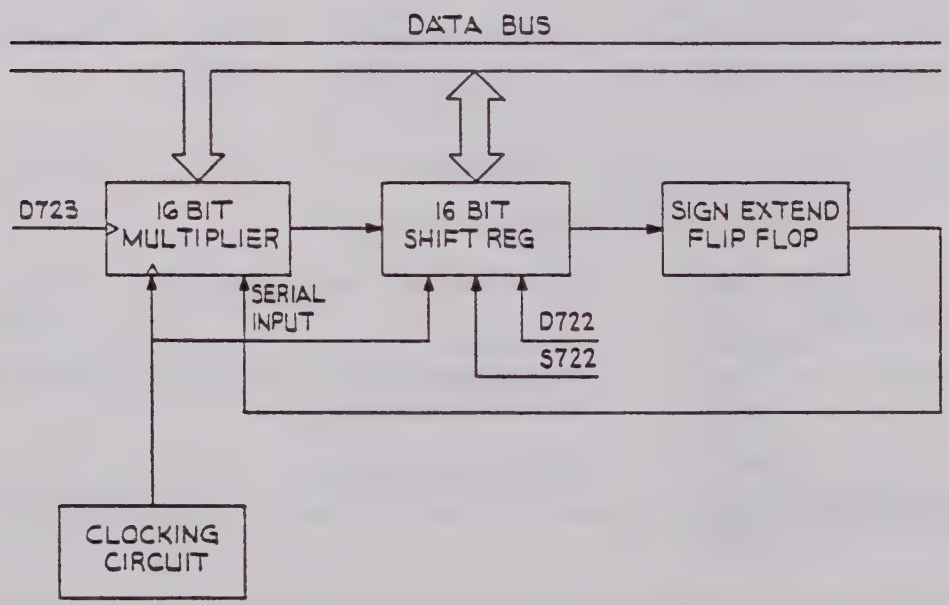


Figure 3-17. Fractional Multiplier Block Diagram

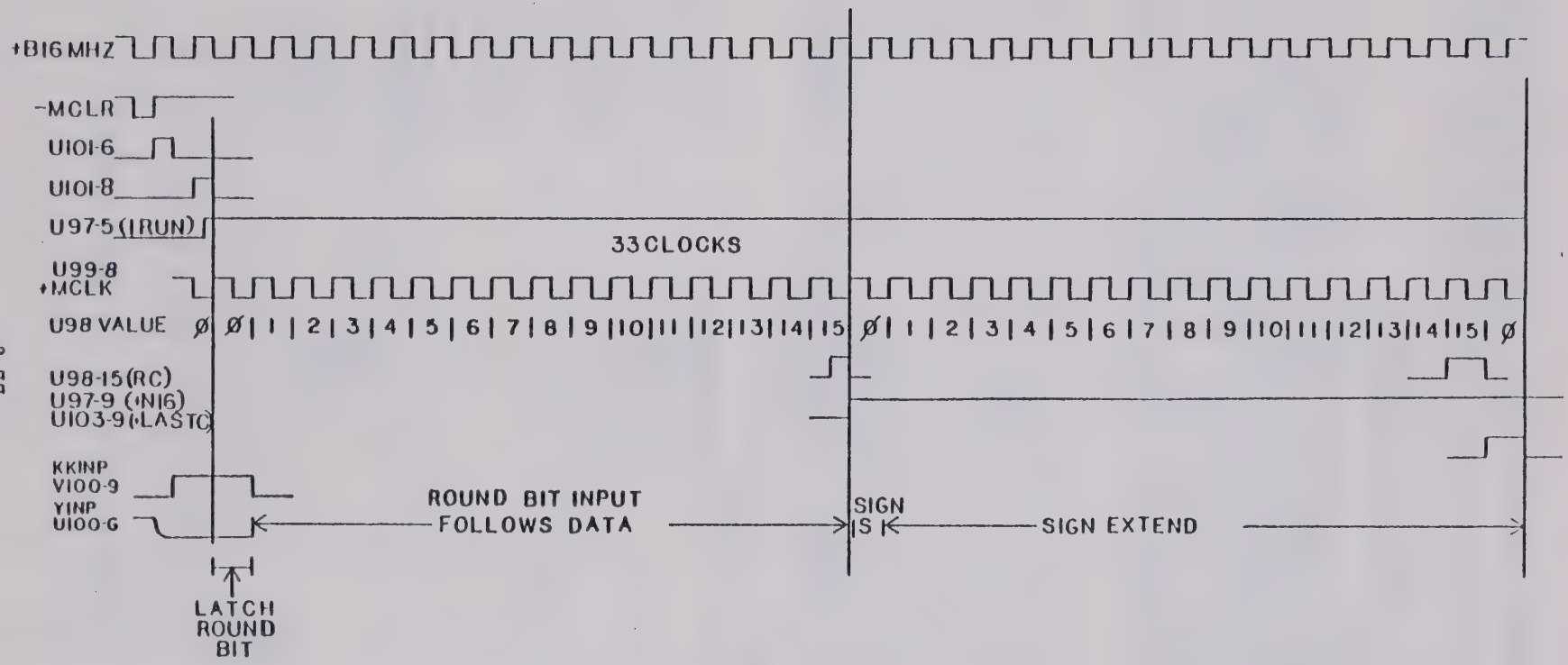


Figure 3-18. Fractional Multiplier, Multiply Timing Chart

3.3.4 Display Board

The following text is primarily referenced to the diagrams listed below:

Block Diagram	Figure 3-19
Detailed Schematic	2510-4702.

The display board provides an interface between the 2501 microprocessor and the keyboard, and the raster scan display and vector generator. The keyboard interface allows the 2501 microprocessor to tell when a key is pressed on the keyboard (by an interrupt only) and identifies the key. The display interface allows the 2501 microprocessor to write vectors into the image memory, which is constantly (60 times per second) sent to CRT monitor by the display board. A 238 line, non interlaced, RS-170 compatible, composite video signal is sent to the CRT monitor via a coax cable from the display board. Most standard TV monitors are compatible with the signal.

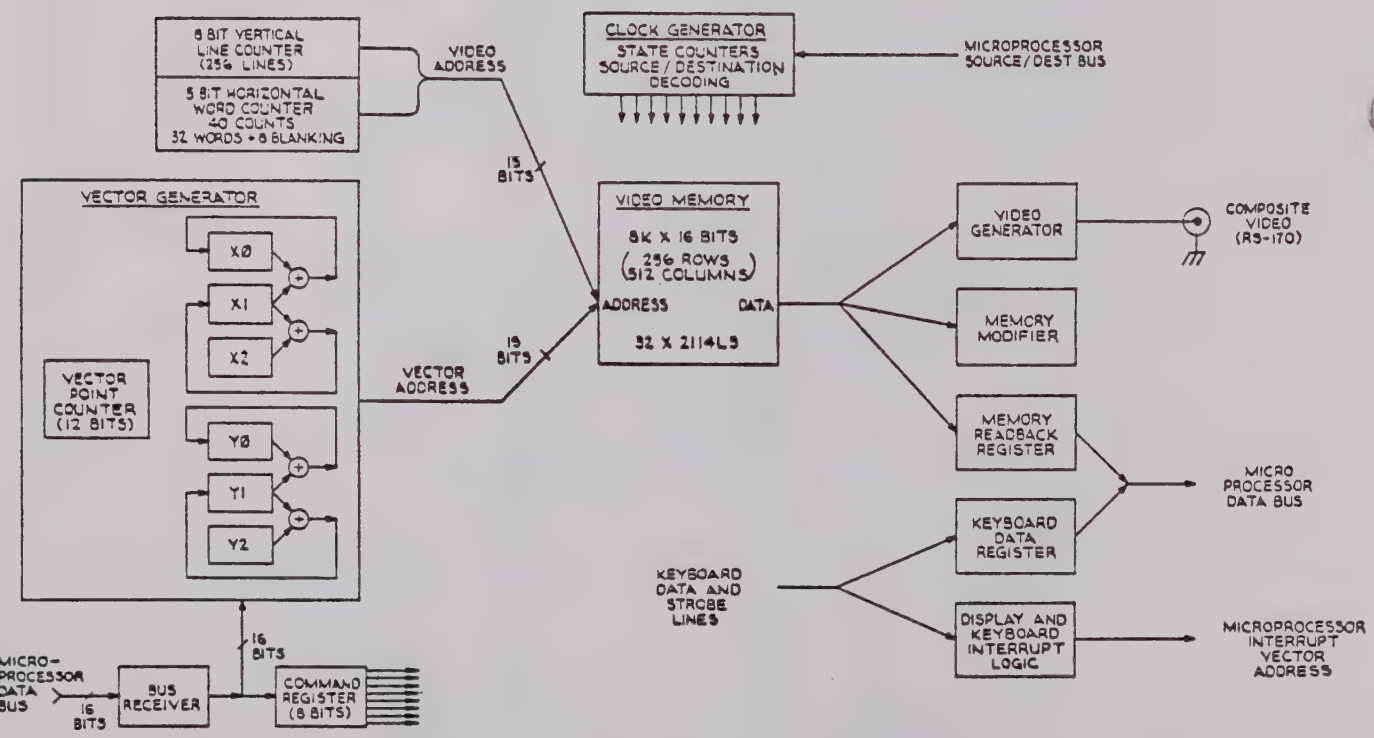
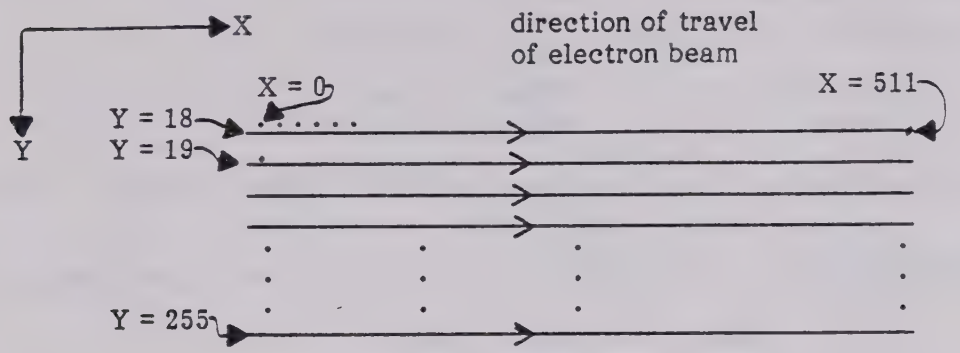
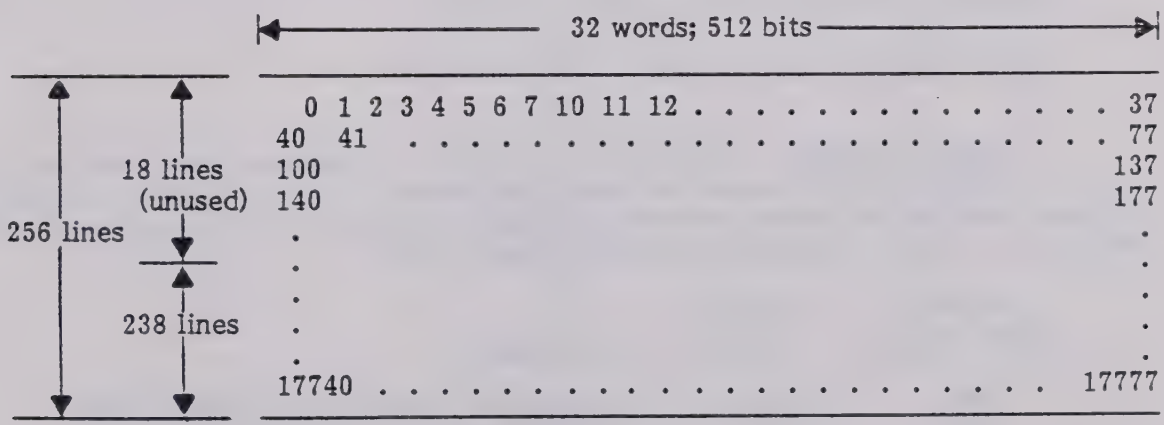


Figure 3-19. Display Board Block Diagram

3.3.4.1 Display General Description. The CRT displays 121,856 dots (512 by 238) with x and y coordinates as shown below:



Only 238 lines are used (instead of 256) so that the entire image can be sent to the screen every 1/60 of a second and still be compatible with any standard TV monitor. This choice also makes the vertical counter very simple. The vertical counter is an 8 bit counter which counts sequentially from 0 to 255 where 0-17 are used for vertical retrace and 18-255 are used for displaying the image memory. (Vertical retrace is the time for the beam to reset from the bottom to the top of the CRT.) The image memory is capable of storing 256 lines. However, the first 18 lines of memory are not used. Memory is 2^{17} bits, organized as 8192 words of 16 bits each. This memory is made up of 32 static RAM chips (2114's) each 1024 words by 4 bits. The correspondence between the memory and the display is shown below:



NOTE

All numbers shown are word addresses (13-bits, in octal). Each division is one word, or 16 display dots. The bits in the memory word are labeled +MD0 thru +MD15 where +MD0 is the leftmost dot and +MD15 is the rightmost dot.

The horizontal counter is a 6 bit, 40 state counter. The first eight states occur during horizontal retrace and for each of the other 32 states one word is sent to the CRT. The counter is connected so as to produce the following sequence on output lines HC0 thru HC5:

0, 1, 2, 3, 4, 5, 6, 7, 32, 33, 34 . . . 61, 62, 63, reset

Horizontal retrace	32 words (1 line0 are sent to the CRT

The dot time was chosen so that all dots are displayed in 1/60 of a second. Thus we have:

DOT FREQUENCY = 60 x 256 x 40 x 16 = 9.8304 MHz = Main Clock Rate

frame rate — vert. count — horz. count — dots per count

DOT (ELEMENT) TIME = $\frac{1}{9.8304 \text{ MHz}}$ = 101.725ns = Te = main clock period

CRYSTAL FREQUENCY = 2 x Dot Frequency = 19.6608 MHz

Some other important numbers we can now calculate are:

LINE TIME = H = 40 x 16 x Te = 640 Te = 65.104 uS

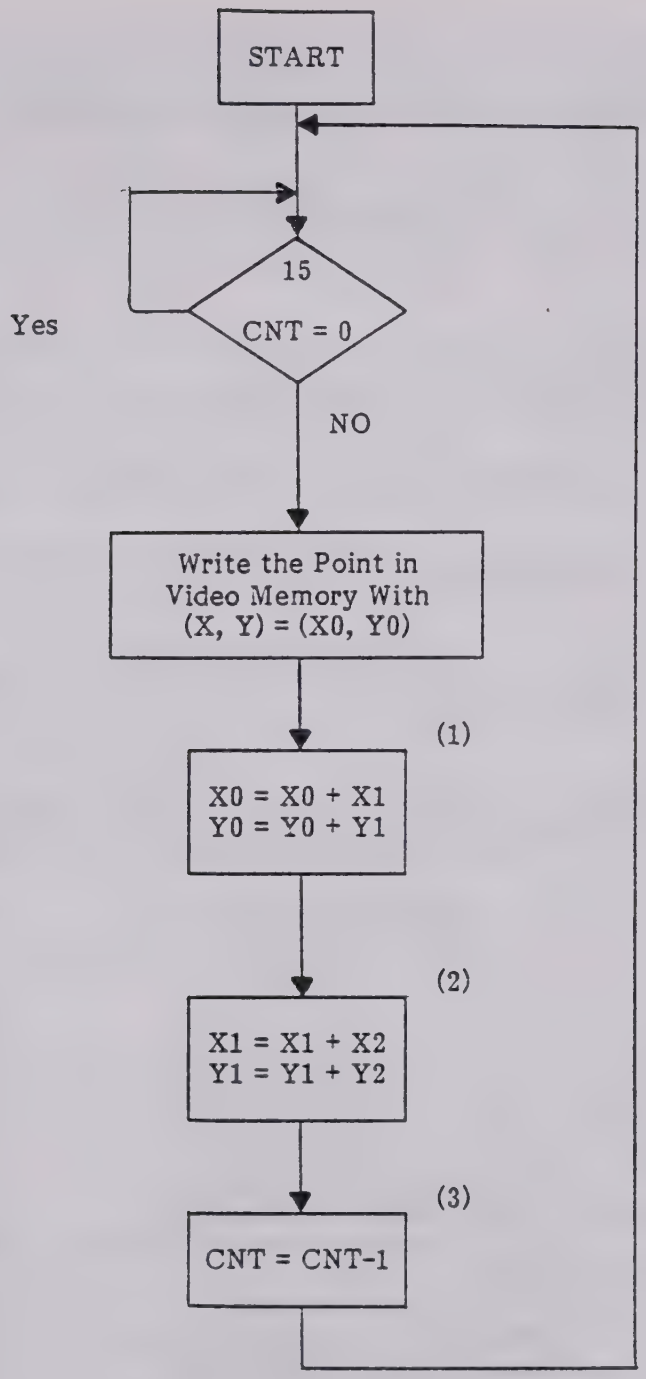
VERTICAL RETRACE TIME = 18H = 1.1719 ms

HORIZONTAL RETRACE TIME = .2H = 13.021 us

Vector Generation. The only way the 2501 microprocessor can enter points into the video memory is through the vector generator. To draw a vector (a straight or curved line) the 2501 microprocessor must load 8 registers in the display controller, each having a separate destination address as noted below:

Destination Address In Octal	Register Name	Function
700	CMD	Command - Selects type of vector write
701	X0	Starting point - X Coordinate
702	Y0	Starting point - Y Coordinate
703	X1	Delta X
704	Y1	Delta Y
705	X2	Delta Delta X
706	Y2	Delta Delta Y
707	CNT	Count - Number of dots in the vector

Any of the registers 700-706 need not be reloaded for each vector if they are known to already contain the desired contents. However, the CNT register must be loaded for each vector, because loading the CNT register starts the vector writing process. The vector writing procedure is shown in the flow chart of Figure 3-20.

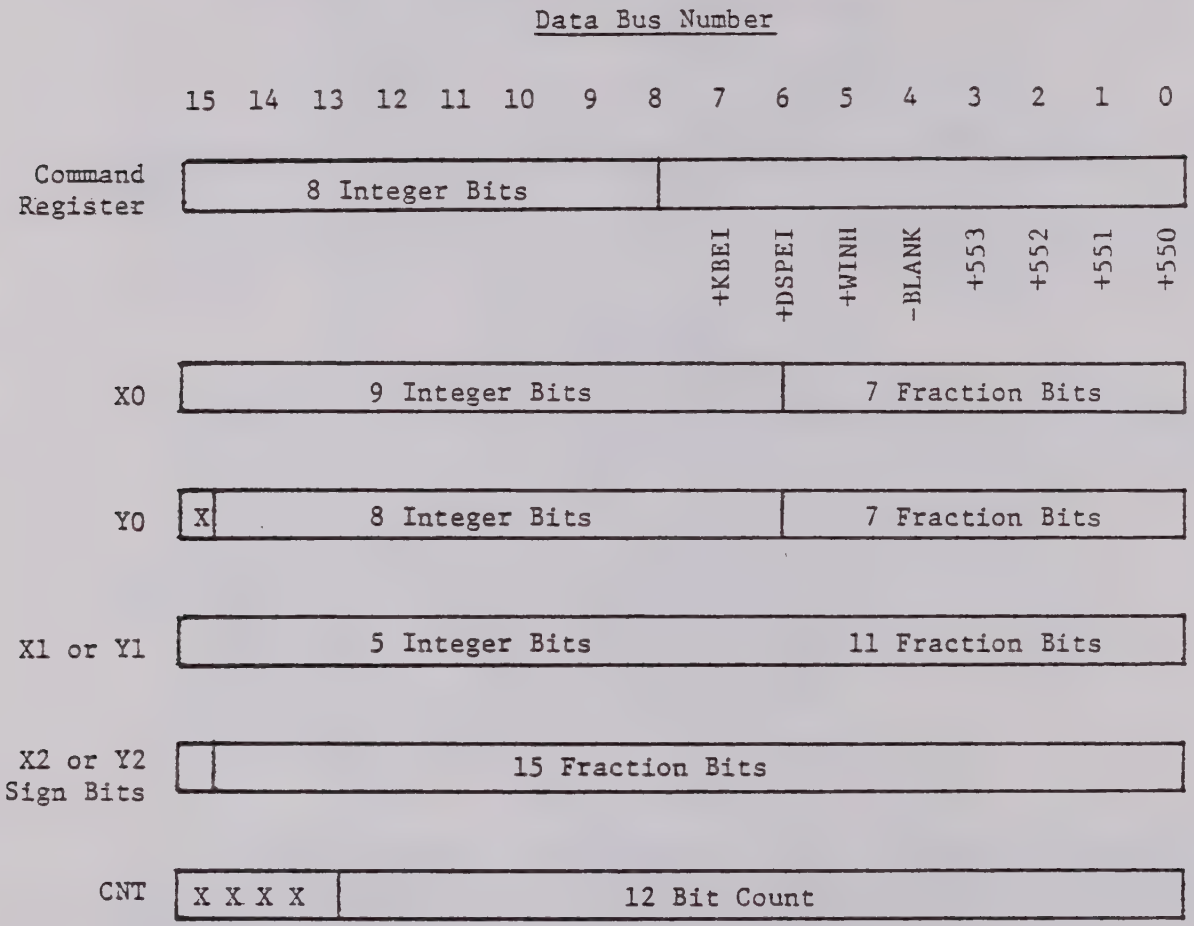


NOTE: The calculations carried out in (1) and (2) are 24-bits long (9 integer bits and 15 fraction bits)

The calculation in (3) is 12-bits long; thus there can't be any more then 4095 dots in a vector.

FIGURE 3-20. Vector Writing Procedure

The eight registers are loaded from the data bus in the following format:



+KBEI	Keyboard Interrupt Enable
+DSPEI	Display Interrupt Enable
+WINH	Write Inhibit - used to provide a memory readback mode (if this is closed up, this line won't slop over)
-BLANK	Blank Screen (not video memory)
550	These bits are used in the
551	Memory Modifier and Video Counter
552	Circuits and are discussed in the
553	Circuit Descriptions later
X	Don't care

Since each dot of the vector write operation usually changes only one bit of one word, both a memory read and a memory write are needed for each dot of the vector. Thus the required word is first read, then the required bit (or bits) are changed, and the modified word is written back to the location in video memory from which it was read. In order to continuously update the display, a read from image memory must occur every 1.628 µs (16 Te) at an address determined by the vertical and horizontal counters. In order to accomplish a vector operation (READ + WRITE) without conflicting with the video read from the same memory, the following 32 state sequence is used for each vector dot that is generated:

S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S
0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14
R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

VIDEO READ	VECTOR READ	VIDEO READ	VECTOR WRITE

813.8 ns

3.255 µs (= 32 Te)

Each division is one clock time (one element time)
Thus our basic vector writing speed is 3.255 µs per dot.

3.3.4.2 Programming Information

The following subroutine erases the entire screen and is used as a programming example, with a line by line explanation below.

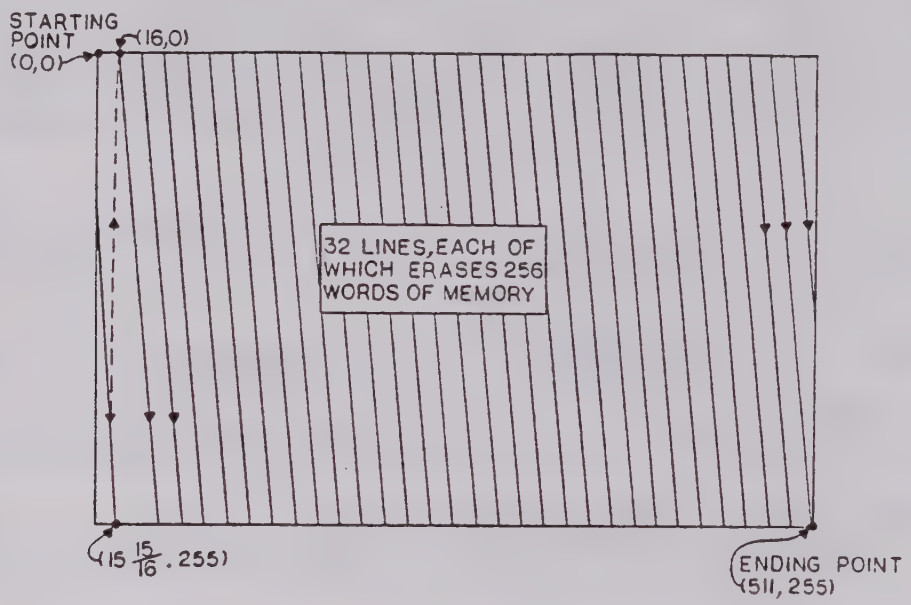
ERASE THE TV TUBE

```
000202  00 000 700 131  ERASE  MOV #0, TCMD      Blank Screen, Set up for erase
000203  00 000 701 131         MOV #0, TX0
000204  00 000 702 131         MOV #0, TY0
000205  00 000 705 131         MOV #0, TX2
000206  00 000 706 131         MOV #0, TY2
000207  10 000 703 001         MOV #0200, TX1    TX1 = 1/16 (S11)
000210  10 000 704 020         MOV #04000, TY1   TY1 = 1    (S11)
000211  00 002 707 131         MOV #2, TCNT
000212  30 652 000 221         JSR  U, WAIT      Wait for TV ready
000213  10 177 707 037         MOV #4095, TCNT
000214  30 652 000 221         JSR  U, WAIT      Wait for TV ready
000215  10 177 707 037         MOV #4095, TCNT   8192 16 Bit Words to Erase
000216  30 652 000 221         JSR  U, WAIT      Wait for TV Ready
000217  10 035 700 001         MOV #0235, TCMD   Unblank,Enable KBINT, allow vector write
000220  04 500 400 134         MOV R0,N,R        Return
```

ROUTINE TO WAIT FOR TV READY

```
000221  00 500 400 134  WAIT   MOV R0 N         Wait 2 instructions before testing
                                                Ready
000222  04 702 000 000         RET TRY           Return if Ready
000223  20 652 000 222         JMP U, .-1        Try Again
```

The basic idea of this routine is to write a vector (in erase mode) which follows the path shown below. Since the erase mode clears a 16 bit wide path, this path will erase the entire screen:



The vector drawn starts at (0,0) and proceeds down to (15-15/16, 255). The next point on the vector would be expected to be 16,256 because the X increment is 1/16 and the Y increment is 1, but since the Y position is only an 8 bit number, this overflows and the next point of the vector becomes 16,0. Since there are 8K words of memory we need this vector to be 8192 steps long. However, the vector point counter can only count up to 4095, so three vectors of lengths 2, 4095, 4095 respectively are written.

Line 202 loads the correct code in the command register for the 16 bit wide erase mode, and also turns off the video so that the viewer will not see the erase take place.

Lines 203 and 204 load the starting point of the vector.

Lines 205 and 206 clear the second derivative terms so that straight lines are produced

Lines 207 and 210 put the X and Y step sizes to 1/16 and 1 respectively.
NOTE: These are loaded as S11 numbers (they have 11-bits following binary point).

Lines 211 and 212 draw the first 2 points of the described vector.

Lines 213 to 216 draw the following 8190 points of the vector.

Line 220 returns to the calling program.

Line 221 is necessary to produce enough delay after loading TCNT so that the display busy flag is valid.

Line 221 tests the busy flag and returns if the vector has been completed.

Programming Considerations. After the TCNT register is loaded, none of the display registers should be loaded until after the vector generator has completed the vector, or unpredictable displays will result. Usually this is done by testing the TV ready bit.

Complementing vectors with an increment of 2 (or more) are ideal for cursors because they are almost always visible and seldom hide what is underneath them. They also can easily be removed by simply re-writing the curser over again.

It should always be rememberd that when a vector is written it will not be seen by the operator instantaneously because of the finite frame time (1/60 of a second). Thus a vector written and immediately erased may or may not be seen. This is especially important when trying to create moving pictures (such as modal displays) and these pictures should be synchronized with the scan time of the TV monitor. This is discussed under the Vector Point Counter circuit description.

3.3.4.2 Circuit Descriptions (Schematic 2501-4702-2D). The following circuit descriptions are arranged generally in order of their appearance on schematic sheets 1 thru 9.

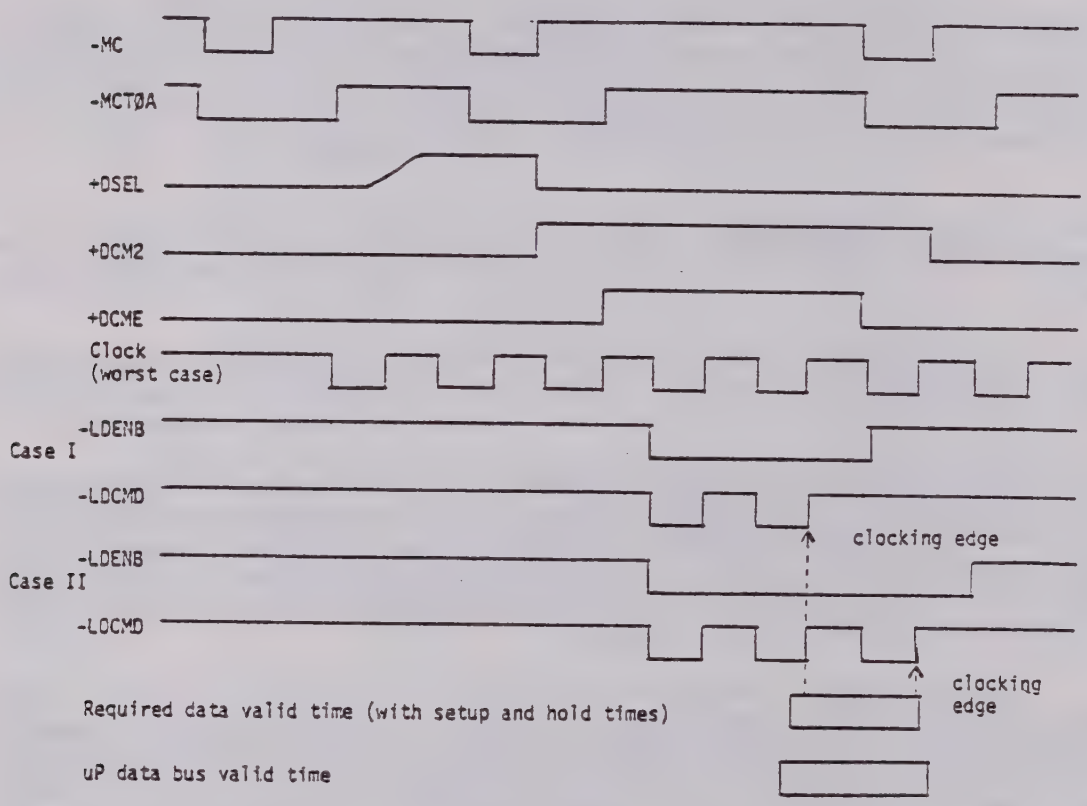
Clock Generator. Inverters U102C and U102E form a 19.6608 MHz oscillator which is divided by two at U113A. If -CLKSTOP is externally forced low, +CLK will follow -SNGLCLK, allowing the circuit to be externally clocked by a board tester.

State Generator. When -INITL is low, all of the outputs of the 32-bit shift register are held low while the serial input is held high because U92A is preset. Since the input to U80 is high, the next clock after -INITL goes high will cause +S0R to go high, clearing U92A and starting a single width pulse moving down the shift register. U92A will set again just as +S15W goes high, causing +S0R to follow +S15W producing a circular loop until -INITL goes low again.

Source Decodes. Source bus lines +S3 thru +S8 are used to form -CNDOE which is active for source codes 700 - 707. Since this signal is used to enable the CONDITION TRUE line of the display board (TRUE means display board ready, FALSE means Display board busy), any of the source addresses 702, 703, 706 or 707 may be used to test the busy status of the display board. Note these are the source codes which are not used for -READBACKOE AND -KEYDATOE, which are decoded by U94B and U94C and then latched during the next master clock by U91C and U91F. For consistency it is suggested that only the preferred source addresses shown below should be used.

Source Address	Preferred Source Address	Name	Function
700,704	700	-KEYDATOE	Read last pushed key of the keyboard
701,705	701	-READBACKOE	Read the last word which was addressed by the vector generator
702,703, 706,707	702	-DSPDONE	True means vector completed.

Destination Decodes. Destination bus lines +D3 thru +D8 are used to form +DSEL which is active for distination codes 700 - 707. +DSEL and +D0 thru +D2 are then latched on the next master clock by U93. The latched signals are resynchronized and decoded by U104 and U105 into 8 signals which are synchronous to the +CLK signal of the display board. These 8 signals are the destination decodes listed in the description of vector generation above. The synchronization with +CLK occurs as follow:



Memory Readback Register. At the end of every vector read operation (end of S6R) U108 and U118 are clocked with the vector data to give the CPU the capability of reading the video memory 16 bits at a time. This would normally be done by loading the desired vector into the vector generator registers and then alternately loading a "one" into the CNT register followed by reading the readback register from the data bus. The word read will be the video memory word which contains the dot that the vector generator had just finished writing. Normally the +WINH (write inhibit) bit of the command register would be set high during a memory readback operation so that the vector generator does not actually insert the specified vector into memory. When the memory readback source code is given, both -READBACKOE and -DBHIGHOE will become active, allowing U108 and U118 to drive the data bus. U118 is also used to drive the most significant byte of the data bus when the keyboard data is read, since the keyboard data only occupies the least significant byte. This is done to insure that the most significant byte of the data bus is not left undriven (in an indeterminate state) when the keyboard data is read (for testing purposes).

Data Bus Receiver. U78 and U116 are tri-state drivers used to drive the A-Bus (A0-15) from the data bus. The A-Bus is used to parallel load the 8 destination addresses of the display controller from the data bus. The A-Bus is also used to load the XA and YA vector registers from the X0 and Y0 registers of the vector generator.

Command Register. The command register is loaded from the low byte of the data bus upon the -LDCMD destination decode (700). Refer to the preceding general description of vector generation for its content.

Vector Generator. The vector generator consists of six 24 bit shift registers whose contents from top to bottom are: X0, X1, X2, Y0, Y1, Y2.

These numbers all have 9 integer bits and 15 fraction bits. X0 and Y0 are always interpreted as unsigned numbers, whereas X1, X2, Y1 and Y2 are treated as signed two's complement numbers. During each dot of a vector generation, all these registers and the serial address shift 25 times while the following computations are being executed.

U17D	X0 = X0 + X1
U17C	X1 = X1 + X2
U17A	Y0 = Y0 + Y1
U17B	Y1 = Y1 + Y2

25 shifts are needed because of the extra delay in the address. U68A and U68B provide a one clock delay so that X2 and Y2 can be recirculated back into the same registers in 25 shifts. U113 starts and stops this shifting operation at the correct times. All of the shift registers are parallel in serial out except for the most significant 16 bits of the X and Y registers which are parallel in parallel out since these need to be read at the beginning of each vector dot cycle.

Vector Point Counter. When the 2501 microprocessor loads the count register (-LDCNT), -DCM2A goes low which clears U70A and B. This causes -DSPDONE and -DSPDONEA to be active indicating the vector generator is in a done state (opposite to what you would expect it to do). However, this done state is only temporary and is necessary to allow the 2501 microprocessor data bus (DB00-15) to be enabled onto the A bus so that the counters can be loaded which occurs on the last rising edge of +CLK when -LDCNT is still low. After the load of the counters has been completed, -DCM2A will go high again, thus allowing U70A to set on the next clock (unless a count of zero was loaded since then -VCNTZERO would remain zero and U70A would never set), thus causing the display to enter the busy state, testable from the condition true line. (Note: this is the reason for the instruction delay required before testing the done after loading the counter since a momentary done state does occur.) Then on the following +S14W, U70B will set, thus disabling the DB bus from driving the A bus and at the same time enabling the vector generator to drive the A Bus. Also on each +S2R of the following N cycles (N is the number loaded into the count reg, a cycle is a 32 state sequence of +S0R to +S15W) +SHF25 will become active causing the vector generator to generate N new display points. The display will remain in the busy state until either the counter down counts to zero (causing -VCNTZERO to become active) or until the 2501 microprocessor executes an instruction that loads any of the display board destination registers. This discussion assumes that +SS13 is inactive. If +SS13 is active, then this circuit acts as a scan synchronizer by causing an interrupt (if enabled) or by driving the condition true line. This works as follows: Assume the display is in the done state. Then the vector point

counter will contain all zeroes, which means that the logic level of the ripple carry output of U71 will be the same as the logic level of the ENT input of U56. Therefore the signal -DSPDONEA follows +VC7 (delayed by 1 clock) and an interrupt can be generated when +VC7 falls (at end of scan) as desired. Also, the condition true line can be tested to determine the state of +VC7. Note that +SS13 keeps -DSPDONE active (through U44C) thus preventing U70B from setting when +VC7 is high.

YA Register. At the end of +S1R, the 8 bit vector "Y" coordinates are loaded into U59 from the Y register of the vector generator. When -VECAOE is active (vector address enable) these 8 bits are sent to the most significant 8 address bits of the image memory.

XA Register. At the end of +S0R, the 9 bit vector "X" coordinates are loaded into latches U58, U109A, and into counter U69. The 5 most significant bits of "X" are sent to the 5 least significant address bits of the image memory when -VECAOE is low. U109 is used to store the bit which indicates which byte (of the word selected by +MA0 to +MA12) will contain the desired vector dot. U69 is used to store 3-bits which indicate which bit of the selected byte will contain the desired vector dot.

Memory Modifier. At the end of +S6R (end of vector read) U96 and U72 are loaded with the memory data at the address chosen by the contents of U59, U58. Then on the 8 clocks which occur at the ends of SR8-15, U96 and U72 get shifted through U95 back into the same position where they were loaded, during which time the vector word gets modified as desired according to the 4-bits +SS0 thru +SS3. For modes 1 and 4 shown in the tabe on the schematic, all 16-bits of the vector data word are modified. For the three modes 2, 3, and 5, only 1 of the 16-bits will be modified. This happens by making the S381 use the B "field" which chooses only one of the two bytes (by U109A) and only one of the 8-bits (by the output of the down counter U69). To see how the correct bit is chosen, suppose we are trying to select bit 3 (the 4th bit). By following the timing diagram (Figure 3-19) notice that +THISBIT becomes active simultaneously with the 4th bit appearing at the input of U95, thus causing only the 4th bit of the selected byte to be modified by the S381.

Video Address Driver. Whenever -VIDAOE is active the memory address bus is driven from the vertical and horizontal scan counters (U63 and U64) so that a memory read will occur at the current screen location.

Memory Write Enable and Chip Select Logic. U74A provides a memory write enable for the vector write starting on +S3W and ending after +S7W provided that -SHF25 is active indicating that the vector generator is activated. The write enable is also inhibited if +WINH (from command register) is active, which is useful when the vector is being used to provide a memory readback operation only. U74B, U68 and U61 will give the correct bank in the memory a chip select signal as shown in Figure 3-19 (see CS).

Memory. The address to output time delay is calculated as follows:

```
  7   S112 (U85)
 34   LS241 or LS374   required stable in 5 clocks = 508 ns
300   2114L3
341 ns
```

Spare delay time = 508-341 = 167 ns

This 167 ns margin is not really spare since all 32 RAM chips tied together will present a 160 pf capacitor load (32 x 5pF max) which will use up approximately 120 ns.

$$T = \frac{CV}{I} = \frac{160\ pF * 5V}{6.5\ mA} = 120\ ns \qquad (6.5\ mA = I_{OH}\ for\ S374)$$

Vertical and Horizontal Counter. (The vertical counter usage has been described in the preceding paragraph on General Display Operation.) The horizontal counter is made up of U76 and U87A and counts in a 40 state sequence. Note that as soon as the counter advances to the eight count (00100) +SETHC5 becomes active which presets U87A and clears U76. This causes the sequence to change from 7 to 32 (00111 - 10000). When the counter counts from 63 back to 0, +HC4 will fall causing the vertical counter to increment by 1.

Video Data Shifter. At the end of +S12R and +S12W the video memory data corresponding to the address generated by the horizontal and vertical counters is loaded into U84, U60. On the following 15 clocks this shift register is shifted right allowing all 16 bits to be presented to the input of the S11 gate. During the second half of each clock period, this data is allowed to pass into the video voltage generator. Thus dots are displayed with a 50% duty cycle. If -BLANK from the command register is low, then no video data will pass through S11 and the screen will be blank. If the line the 16-bits of this register are shifting out is parallel with a horizontal or vertical blanking interval, then +SYNCENB (sync enable) would have been active during +S12R or +S12W so that the shift register would get cleared by U88B thereby presenting a blanked video level to +TTLVIDEO.

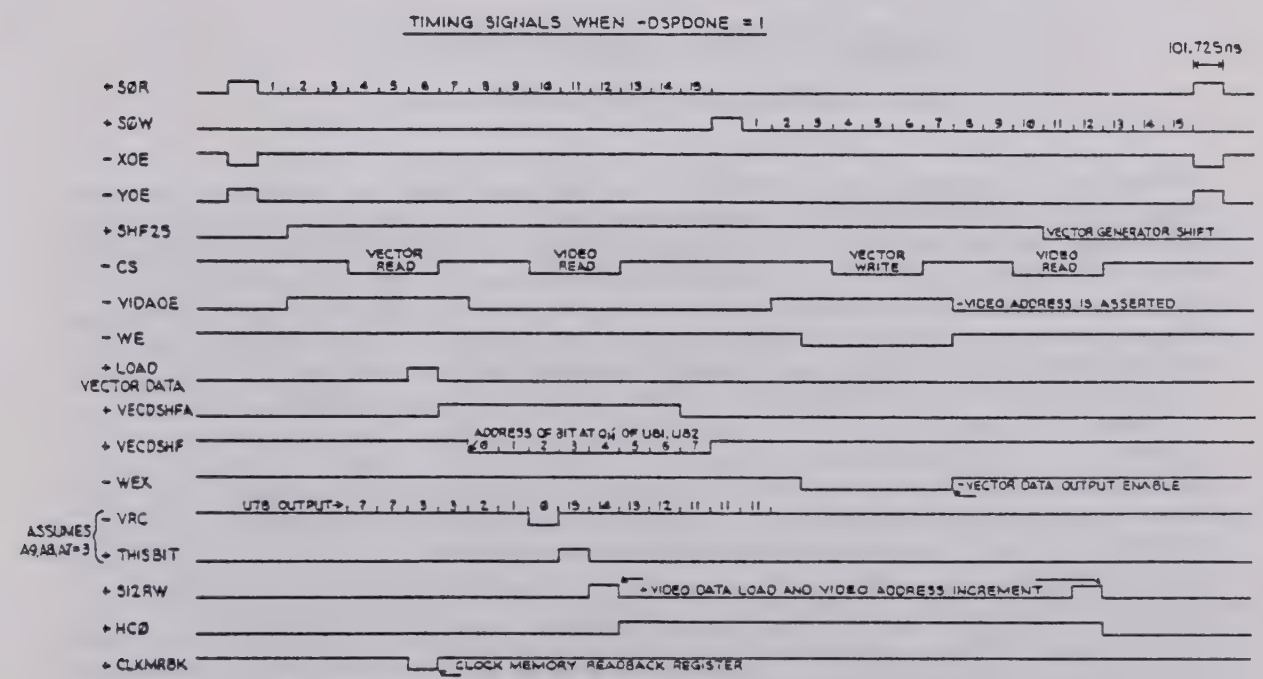
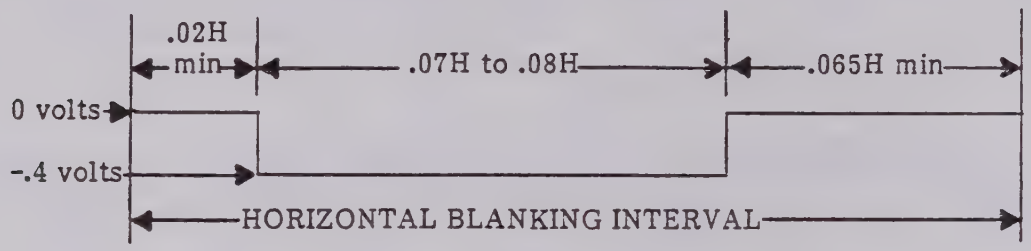


Figure 3-21. General Display Timing Diagram

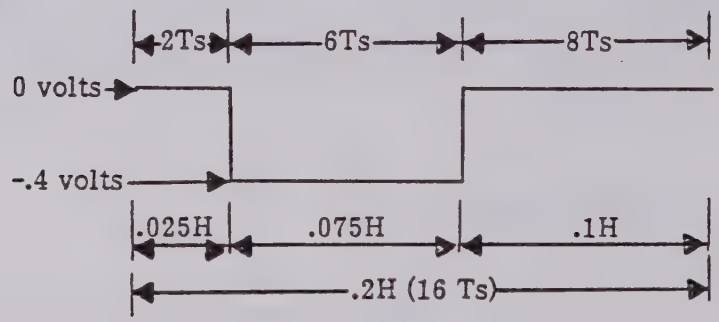
Sync Generator. To adequately describe the sync generator we must identify the sync requirement of the composite video. The element time for sync generation (Ts) was chosen to be 8 times as long as the video element time. Thus we have:

$$T_s = 8\,T_e = 8\left(\frac{H}{640}\right) = \frac{H}{80} = .0125H$$

The requirements for the horizontal sync time are as follows:



The sync pulse which is generated by the display controller was chosen to be as follows:



The ability to generate the 3 different sync patterns each one scan line in length, (called SYNCA, SYNCB, SYNCC - see Figure 3-20) can satisfy all of the requirements for horizontal and vertical sync generation. The output of U110 (+SYNCL) which is buffered before being sent to +TTLSYNC will always be one of the 3 sync signals mentioned — the choice being dependent only on the state of the vertical counter. The scheme is as follows: The first 3 scan lines are SYNCA (this is the beginning of vertical retrace). The following 3 scan lines are SYNCB. The following 3 scans after that are again SYNCA. Then all of the remaining 247 scans are of the type SYNCC. Of these 247 lines, the first 9 occur during the vertical blanking period and the following 238 lines occur while video data is being sent to the CRT. Note that the SYNCC scan line provides the proper horizontal sync pulse shown above. When +HC5 (from the horizontal counter) then U88A output will be high (+SYNCENB). Thus we see that the first 8 counts out of 40 from the horizontal counter are forced to be horizontal blanking, thus fixing the horizontal blanking interval to be $\frac{8}{40}H$ or .2H as desired. +SYNCENB will also be active whenever U87B is set, causing the vertical blanking period. Thus the vertical blanking begins as +VC7 falls (i.e., when the counter counts back to zero) which sets U87B and ends at the beginning of the 19th line (line no. 18) which is the first time both +VC4 and +VC1 are high.

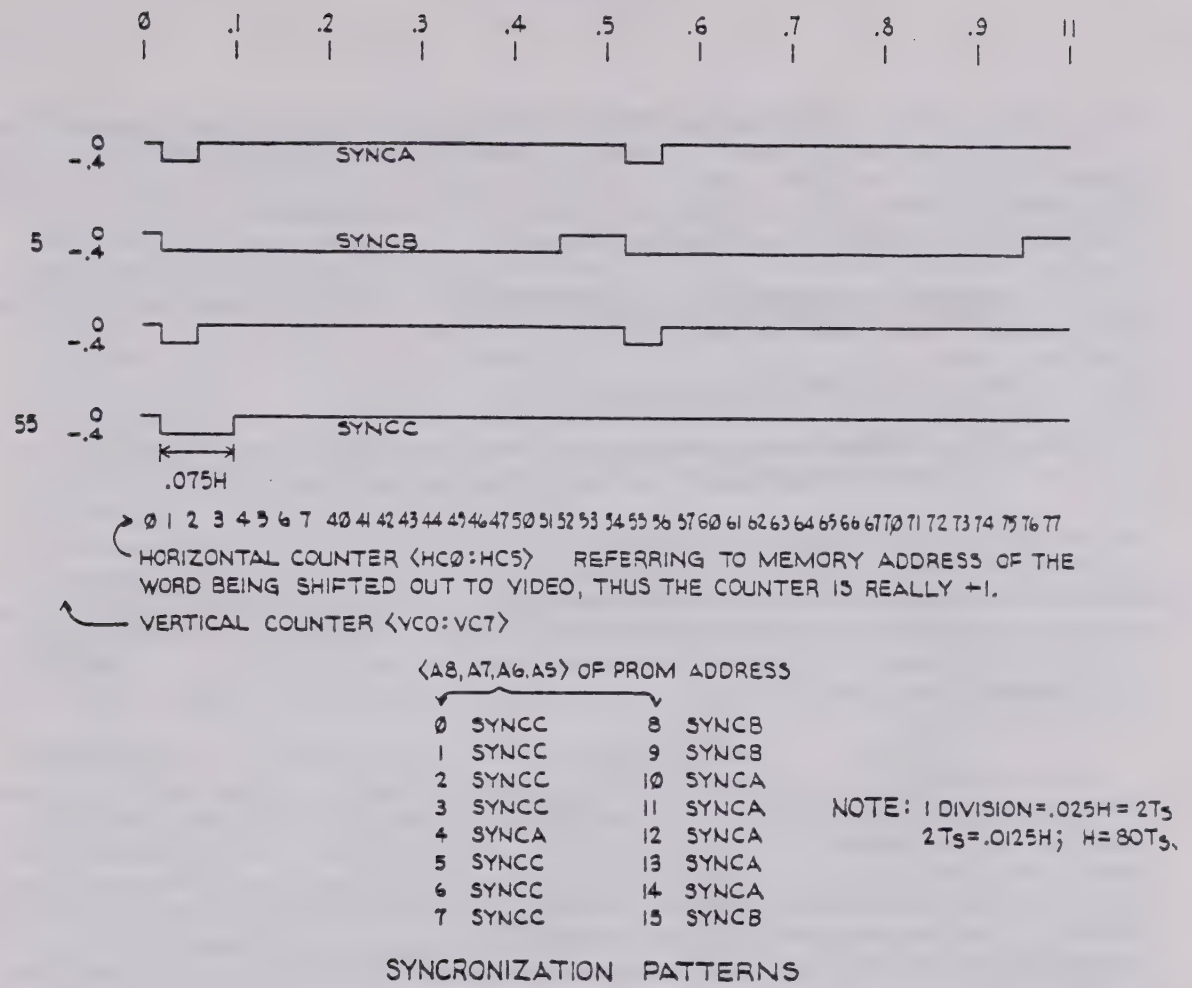

Ø .1 .2 .3 .4 .5 .6 .7 .8 .9 1
0 -.4
SYNCA
5 0 -.4
SYNCB
0 -.4
55 0 -.4
SYNCC
.075H
Ø 1 2 3 4 5 6 7 40 41 42 43 44 45 46 47 50 51 52 53 54 55 56 57 60 61 62 63 64 65 66 67 70 71 72 73 74 75 76 77
HORIZONTAL COUNTER (HC0:HC5) REFERRING TO MEMORY ADDRESS OF THE WORD BEING SHIFTED OUT TO VIDEO, THUS THE COUNTER IS REALLY +1.
VERTICAL COUNTER (VC0:VC7)
(A8,A7,A6,A5) OF PROM ADDRESS
Ø SYNCC
1 SYNCC
2 SYNCC
3 SYNCC
4 SYNCA
5 SYNCC
6 SYNCC
7 SYNCC
8 SYNCB
9 SYNCB
10 SYNCA
11 SYNCA
12 SYNCA
13 SYNCA
14 SYNCA
15 SYNCB
NOTE: 1 DIVISION=.025H=2Ts
2Ts=.0125H; H=80Ts.
SYNCRONIZATION PATTERNS

Figure 3-22. Sync Timing

As can be seen in Figure 3-22, for each scan line we must generate 80 sync elements (2 elements per horizontal count). Therefore U110B is clocked at +S12R and +S12W (when the horizontal counter is incremented) and also at +S4R and +S4W (the midpoints between counts). The contents of the PROMS are chosen so that +SYNC (the output of the LS253) when latched by U110B will produce the desired waveforms shown in figure 3-20. +SYNC is essentially a function of the following variables: -V3, -V2, +VC1, +VC2, +HC5, +HC4, +HC3, +HC2, +HC1, +HC0, and +VIDAOE.

Composite Video Voltage Generator. If the blanking level is defined as 0 volts then the sync level should be -.4 volts and the white level should be between .4 and 1.0 volts. The two resistors feeding the grounded base transister (Q1) implements a current summer which passes through the 300 ohm resistor to generate either the sync level or the white level or the blanking level, depending on whether +TTLSYNC or +TTLVIDEO or neither (respectively) is high. +TTLSYNC and +TTLVIDEO are never to be high at the same time. The dc level at the collector is irrelevant since this signal is capacitively coupled to the output amplifier, therefore only the correct voltage changes must be made (at the collector) between the 3 desired output levels (BLANKING, WHITE, and SYNC). The LH0002 is a unity gain amplifier used to provide

low output impedance without sacrificing the fast rise and fall times needed. The -15V is regulated and filtered to provide a clean -5V for the LH0002. The +5V is filtered both for the LH002 and for the S11 buffer which drives the video voltage generator. This was done to reduce the effects on the displayed image of digital signal noise being injected into the composite video.

Keyboard and Display Done Interrupt Logic. The display board interrupts the 2501 microprocessor on either of the following events:

- A keyboard key has been hit, or
- A vector has been completed by the vector generator (i.e., CNT=0) or +VC7 has fallen when code 13 has been selected.

In the first case, a negative going edge at the keyboard +STROBE input causes the 8 keyboard data lines to latch into U101 causing U90A to set which causes the interrupt request signal (-IR4) to become active on the next microprocessor clock (+MC). The interrupt will remain pending indefinitely until the grant signal (+IG4) becomes active. Then at the beginning of the next +MC, U91C will turn on for one master clock period, thus enabling the interrupt vector through U114. The interrupt vector asseted on +IV0-7 (201 octal).

The sequence for an interrupt from the vector generator is identical except that the falling edge of -DSPDONEA will begin the sequence instead of +STROBE and the interrupt vector asserted is 200 instead of 201. Both interrupts may be pending at the same time in which case both U90A and U90B are set. In this situation when the grant comes, vector 201 will be enabled, effectively giving the keyboard interrupt a higher priority. When the keyboard interrupt routine reads the keyboard data, -KEYDATOE will cause U90 to clear, but -IR4 remains active. Thus when the program returns from the keyboard interrupt routine another grant will cause vector 200 to be enabled and control will pass to the DSPDONE service routine. This service routine should clear its interrupt flip-flop (U90B) by loading any display register (-DCM2A) or by toggling +DSPEI. Note that if a grant comes when neither interrupt is pending, then +IG40 will become active, thereby passing the grant to the next device in the chain hooked up to this interrupt priority (level 4).

3.3.5 **Universal Interface Board** (Block Diagram Figure 3-21, Schematic 2501-4703-2D)

The Universal Interface board consists of three functionally distinct parts — the slave interface, interrupt interface, and non-processor request (NPR) interface. The slave interface enables the 2501 microprocessor to respond to requests from the PDP-11 for data transfers. This allows the 2501 microprocessor to emulate the DEC Extended Arithmetic Element (EAE). The interrupt interface allows the 2501 microprocessor to cause an interrupt of the PDP-11. The slave interface in conjunction with the interrupt interface allows the 2501 microprocesssor to emulate the DL11 interface to provide console terminal service in lieu of other terminals such as DEC writer or TEK 4010. The NPR interface allows the 2501 microprocessor to perform transfers to and from memory or other devices on the PDP-11 Unibus without intervention from the PDP-11 processor.

3.3.5.1 **Slave Interface.** Four sets of unibus addresses are decoded for use with the slave interface. (Jumpers are used to allow alternate addresses.) The addresses are as follows:

Standard Use	Unibus Address	Alternate Address	Notes
4010	777560-777566	763560-763566	DL11 registers - Controls the 4010
EAE	777300-777316	777320-777326	EAE registers
FFT	763500-763576		Used for all PDP-11 computations which are done or aided by the microprocessor
EXTRA		760000-767776	Used to emulate an unplanned unibus device in the future (possibly for the real time clock)

When one of the above addresses is used on the Unibus, the 2501 microprocessor is interrupted (Level 7) at an address determined by the interrupt vector mapping logic (Table 3-9). During a write to slave operation, the Unibus data lines are read directly to the microprocessor data bus by the 2501 microprocessor, thus producing the slave sync. During a read from slave operation, the 2501 microprocessor will load the data into the slave data register before initiating the slave sync. In both cases the slave sync ends when the trailing edge of the master sync is seen, thus completing the slave operation. However the 2501 microprocessor can prevent the slave sync from ending at this time so that the slave operation can be terminated at a later time. This is used to avoid a possible problem with the timeout delay during the EAE emulation.

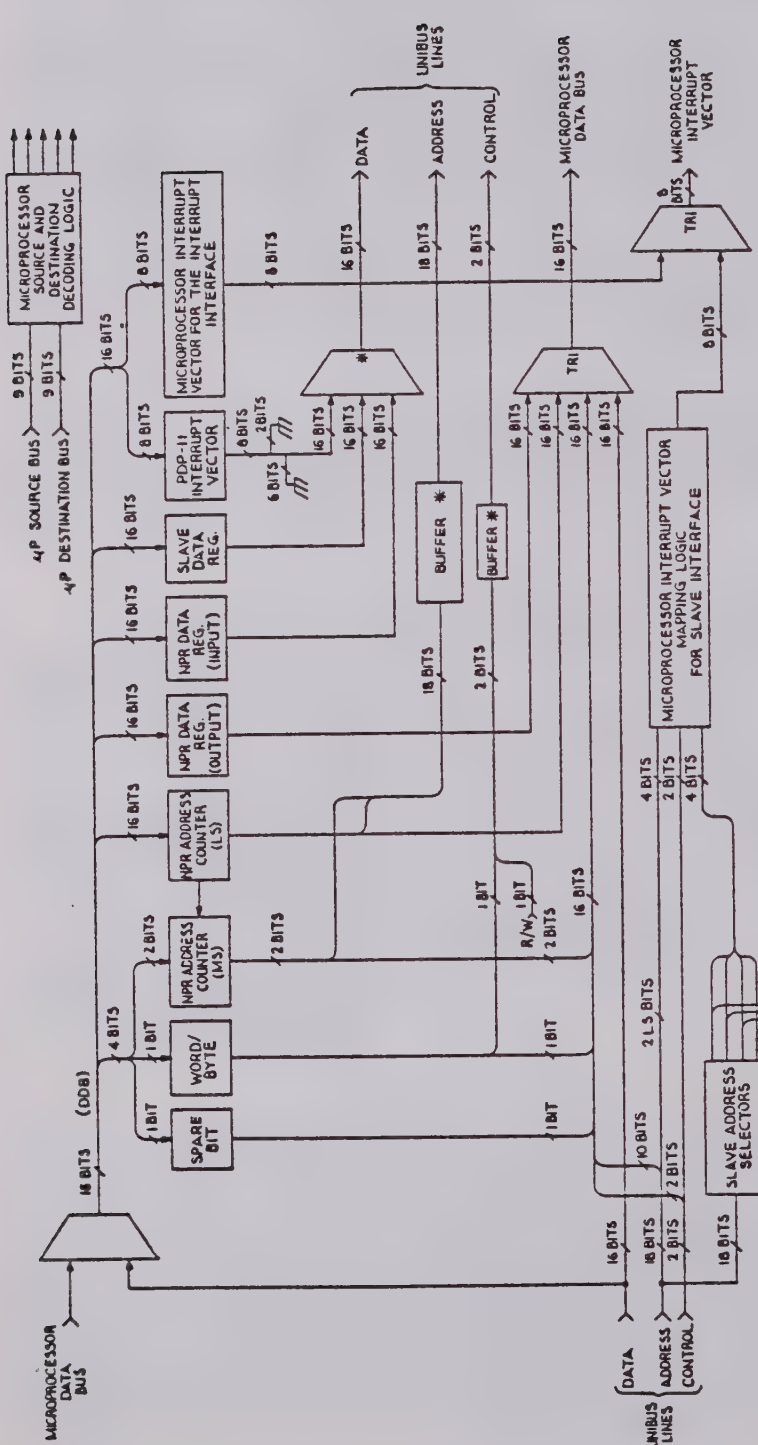


Figure 3-23. Unibus Interface

The source and destination codes used for the slave interface are as follows:

CODE	NAME	USE AS SOURCE	USE AS DESTINATION
350	UB	Read bus data as slave	Write bus data as slave; Complete slave sync if inhibited
351	UBI	Same as UB, but also inhibit end of slave sync.	Same as UB, but also inhibit slave sync
364	UA1	Read Unibus Control bits (C0,C1) and the 10 LS bits of the Unibus Address	

TABLE 3-9. Interrupt Vector Mapping Logic

Device	Interrupt Vector		16	8	4	2	1
4010 Emulation	20-37	Least Significant 4-bits are:		AD2	AD1	L1	L0
EAE Emulation	40-77	Least Significant 5-bits are:	AD3	AD2	AD1	L1	L0
Interface I	100-137	Least Significant 5-bits are:	AD3	AD2	AD1	L1	L0
Interface II	340-377	Least Significant 5-bits are:	AD3	AD2	AD1	L1	L0

L1	L0	Operation
0	0	Transfer a word from master to slave
0	1	Transfer the low byte from master to slave
1	0	Transfer the high byte from master to slave
1	1	Transfer a word from slave to master

The Unibus slave operation begins with the rising edge of the master sync pulse (Figure 3-24). Unless a previous slave operation has just been completed, +SYNCR will be high, allowing U31A to set on the next master clock (MC), causing -IR7 to go active. Unless the 2501 microprocessor is at priority level 7, the interrupt grant will be received right away as shown in Figure 3-24. If the 2501 microprocessor's priority is 7, then +IG7I will not go high until its priority is lowered. Upon receiving +IG7I -ENBSLVEC (enable slave vector) will go active at the next MC causing U89 to send the proper interrupt vector to the 2501 microprocessor (see Table 3-9).

Transfer from Master to Slave. (i.e., from Unibus to 2501 microprocessor) (DC1=1). Once the 2501 microprocessor is in the interrupt routine, it can receive data from the Unibus by using an instruction such as: MOV UB,R0 in which case the Unibus data will end up in R0. The signal +SREAD is a latched source code resulting from this instruction. The master clock edge which ends +SREAD, clocks the Unibus data into the Am 2901 and also sets U30B, causing -SYSN01 to go active, making +SSYN0 go high about 100 ns later. When the master sees the slave sync (+SSYNO) go high it responds by lowering the master sync pulse. This causes -RESLAVE to go low (because -SYNCINH = HIGH) which triggers the 9602 one shot causing -SYNCRD to go low. 3 μs later -SYNCRD will go high again causing +SYNCR to go high which then allows another 2501 microprocessor interrupt to occur if +SELS becomes active again. +SELS may become active before the 3 us timeout has been completed, (see Figure 3-25) but +SYNCR being low prevents U31 from setting until after the 3 μs timeout. This delaying of -IR7 would only be likely in the event that the PDP-11 requests a slave operation from the 2501 microprocessor in two consecutive instructions. This timeout delay is used to prevent the possibility of the 2501 microprocessor getting completely tied up in the interrupt service routine for the slave interface. This could happen for instance if the PDP-11 was executing the following code for the purpose of detecting a key strike from the operator:

```
WAIT:  TSTB  @#177560   ;Is receiver done?

       BNE   WAIT       ;If not, test again.
```

Transfer from Slave to Master. (i.e., from microprocessor to Unibus) (DC1=0; DC0=0). Once the 2501 microprocessor is in the interrupt routine, it can send data to the Unibus by means of an instruction such as: MOV R0,UB in which case the data in R0 is sent to the Unibus. The signal +WRUBL is a latched destination code resulting from this instruction. When the instruction ends, +WRUBL and -SYSN02 will fall, thus enabling the 2501 microprocessor data onto the Unibus (see Figure 3-24). About 100 ns later +SYSN0 goes high telling the PDP-11 that the data is ready (the delay of +SYSN0 is to satisfy Unibus timing restrictions for deskew — at least 75 ns of deskew is required. The master will respond to the slave by lowering the master sync after it has received the data. The slave sync will then go away in response to the falling master sync, also causing -SYNCRD to go low for 3 μs thus preventing another slave operation during that time, as described above.

Note that although not shown in Figure 3-24 the 2501 microprocessor may use the instruction MOV UA1, XXX to get the seven least significant address bits of the slave operator (AD0-AD6) and the two unibus control bits DC0 and DC1.

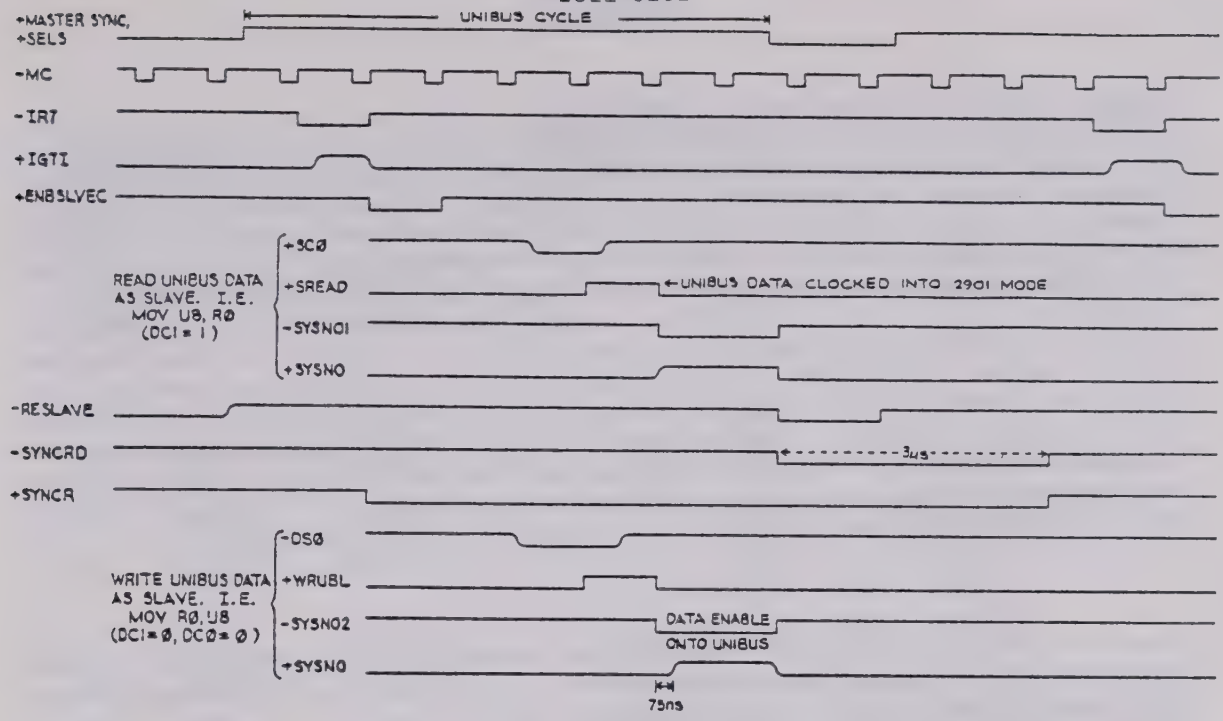


Figure 3-24. Slave Interface Timing Read/Write

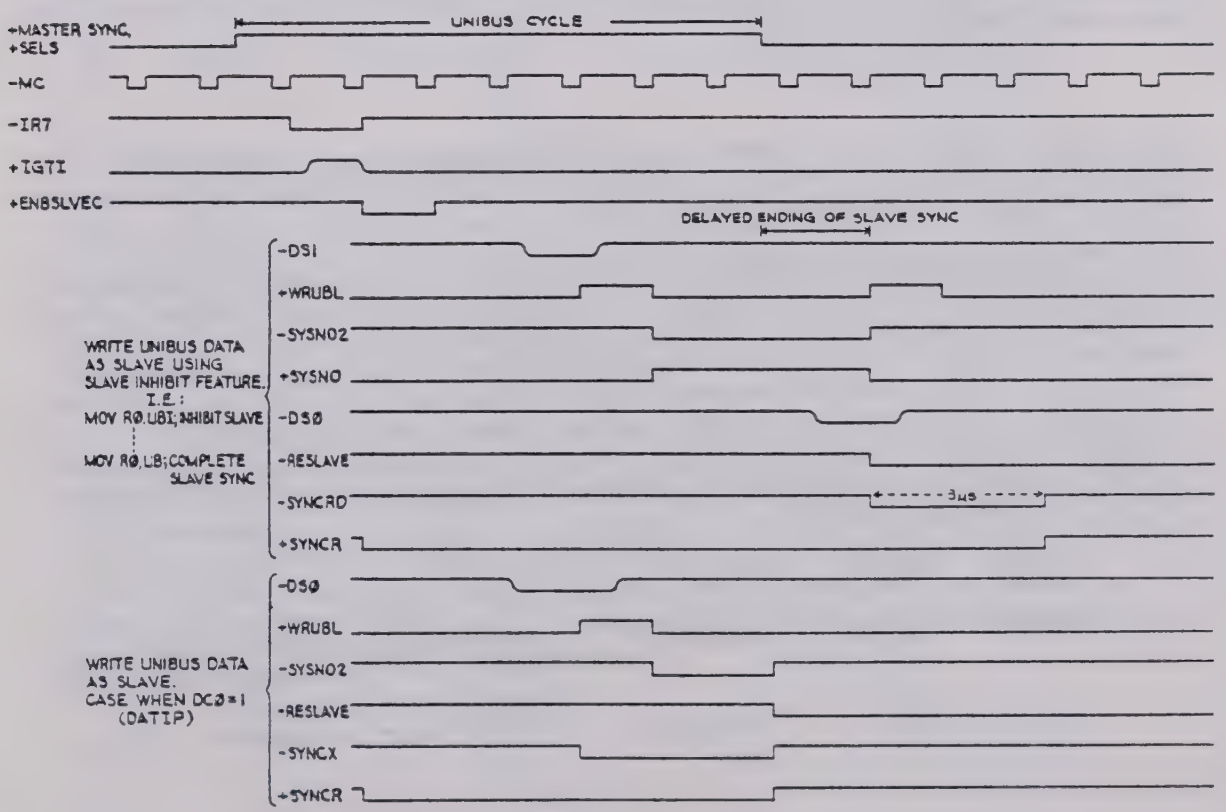


Figure 3-25. Slave Interface Timing - Sync Inhibit and Data In Pause

Transfer from Slave Using Slave Inhibit Feature. The need for this feature arises from the following problem. All Unibus devices which act as a slave must respond to the master sync within 10-20 μs (depending on model of PDP-11) or the PDP-11 wil execute a time-out trap indicating that the device is non-existent or not functioning. During an EAE emulation, if the 11 code requested the result of a multiply immediately after sending the multiplier, the 2501 microprocessor would not be able to compute the product and respond to the master sync within the required timeout delay period. To prevent this problem, when a multiplier is sent to the EAE MQ register, the 2501 microprocessor reads the multiplier from the Unibus using the slave inhibit feature. The effect of this is that the 2501 microprocessor receives the multiplier, raises the slave sync and leaves it high thus preventing the next PDP-11 instruction from starting, which allows the 2501 microprocessor enough time to compute the product. The 2501 microprocessor may hold the slave sync high for as long as desired without violating any Unibus timing restrictions. To read the Unibus in this manner, the 2501 microprocessor would use the following instruction:

```
MOV UBI, R0
```

Once the 2501 microprocessor has completed enough of the work so that it could respond quickly enough to the following PDP-11 instruction, the 2501 microprocessor can release the slave syn by means of an instruction such as:

```
MOV R0, UB
```

The only effect of this instruction is to lower the slave sync if the slave sync has been uninhibited. The 2501 microprocessor may also write to the Unibus and inhibit the slave sync by using the instruction:

```
MOV R0, UBI
```

The timing for this type of transfer is shown in Figure 3-23. The signal -DS1 is the destination decode which initiates the transfer and -DS0 is the destination decode which initiates the completion of the slave sync.

3.3.5.2 Unibus Interrupt Interface. The 2501 microprocessor stores a word in the interface interrupt register to initiate an interrupt in the PDP-11. The upper byte of the stored word contains the 11-address of the interrupt (bits 2-9). The lower byte contains the address of an interrupt vector in the 2501 microprocessor. After the 11 interrupt is complete, the 2501 microprocessor is interrupted by the Unibus interface. A condition code, testable by the 2501 microprocessor, indicates whether or not the interrupt interface is busy, i.e., if the interrupts of the PDP-11 and of the 2501 microprocessor have been completed. The following source and destination codes are used for the interrupt interface:

Code	Name	Type	Use
352	UBINT	Destination	Store interrupt vectors for the PDP-11 and the microprocessor and begin interrupt sequence.
352	UIC	Condition Code	True if interrupt interface is busy.

3.3.5.3 Non-Processor Request Interface (NPR). Word or byte transfers are accomplished through the NPR data register at an address determined by the contents of an 18-bit address counter. This address counter can be automatically incremented so as to minimize the number of microprocessor instructions needed to perform a block transfer. This interface is fully interruptible (i.e., all registers which the 2501 microprocessor can write into can also be read). The following source and destination codes are used with the NPR interface:

CODE	NAME	TYPE	USE
353	UA0	Source & Dest	Lower 16 Bits of NPR Address Counter
354	UA1	Source & Dest	Upper 2 Bits of NPR Address counter
354	UA1	Source	Unibus Control Bits (C0,C1); 10 LS bits of Unibus Address
355	UD	Source	Read Unibus NPR Data Register
355	UA0R	Dest	Store in UA0 and Begin NPR Read
356	UDW	Dest	Store in NPR Data Reg and Begin NPR Write
357	UDIW	Dest	Same as UDW but Increment the NPR Address Counter First
356	UDIR	Source	Read Unibus Data Reg; Increment the NPR Address Counter; Start NPR Read
375	UBR	Condition Code	True if Unibus Interface is Ready

3.3.5.4 Unibus Interface Initialize - Power Up. The PDP-11 transmits an initialize pulse on the Unibus upon powerup, or when the PDP-11 executes a reset instruction. The length of the initialize pulse (INITL on the Unibus) varies between 20 ms and 100 ms, depending upon the model of PDP-11. The Unibus interface board receives this pulse and generates a much shorter pulse (about 15 μs) which begins at the leading edge of the Unibus initialize pulse. This shorter pulse is connected to the 2501 microprocesor initialize line and causes a reset of all the boards on the 2501 microprocessor bus (including the Unibus card).

The 20-100 ms period between the end of the microprocessor reset and the end of the PDP-11 reset allows the 2501 microprocessor to initialize itself before the PDP-11 demands attention from the 2501 microprocessor. During this time the 2501 microprocessor must not demand attention from the PDP-11 by initiating an NPR or interrupt of the PDP-11. The 2501 microprocessor can determine if the PDP-11 reset is completed by reading bit 15 of UA2 in the Unibus interface. This bit will be '1' if a reset is in progress, otherwise '0'. It is advisable to wait 10 microseconds after the PDP-11 reset ends before demanding attention from the PDP-11.

Effect of Microprocesor Reset. In general most registers are cleared and the 2501 microprocessor starts executing instructions at location zero. A board by board analysis of the effect of the reset follows:

CPU Board

Instruction counter	- Cleared
Subroutine stack pointer	- Cleared
Priority register	- Set to priority 7
Map register	- Unchanged
Status Register	- All bits set to '1'
Condition true flip-flop	- Set to TRUE (Result: if the instruction in location 0 is a conditional jump, etc., it will see a true condition)
Subroutine stack contents	- Unchanged
R0-R15, Q 2901 Registers	- Unchanged

PROM Board

Stack Pointer	- Unchanged
Index Register	- Unchanged
Scratchpad Contents	- Unchanged
Real Time Clock (SH0)	- Cleared
Compare Register (D660)	- Cleared
Clock hold register 8 bits (S720)	- Unchanged
Upper 8 bits S720,S667	- Not affected, reflect inputs
I0-I3 (S667)	- Cleared
CI0-CI3 (S667)	- Not affected, reflect inputs
(D667) 16 bits	- Cleared
(D720) least 8 bits	- Unchanged
(D720) bits 8-13	- Cleared
Printer heater enable	- Disactivated (HC1 cleared)
Multipler (D723)	- Unchanged
Multiplier (D722) (S722)	- Cleared
Multiplier run (S7203)	- Set to not running

NOTE

A multiply in progress is aborted by reset.
Real time clock interrupt request - canceled by reset

Display Board

Raster memory contents	- Unchanged
Six vector generator registers	- Cleared
Command register	- Cleared
Vector point counter	- Not affected or unpredictable
Display done condition	- Initially set to done but then set to not done if TCNT is non-zero

Display readback register	- Not changed
Vertical counter	- Cleared (Breaks up raster)
Keyboard data register	- Unchanged
Display done interrupt request	- Cleared
Keyboard character ready interrupt request	- Retains previous state

NOTE

To completely reset the display board the microprocessor must clear TCNT and read the keyboard data register.

Unibus Interface Board

Slave interface interrupt request	- Cleared
Slave interface slave sync out	- Cleared (if master sync from unibus not asserted)
Interrupt interface microprocessor interrupt request	- Cleared
Interrupt interface register	- Unchanged
NPR interface NPR request	- Cleared
NPR interface Unibus address vector VA0, VA1	- Cleared
NPR interface data register	- Unchanged

CHAPTER 4

MAINTENANCE

The principal tools for testing and service of the 2511/2514 system are the diagnostic programs of the diagnostic software package. The diagnostic programs, procedures, and troubleshooting hints are described in detail in the separate volume 2511/2514 Systems Diagnostic Manual, Form No. 2511-0690. The user should be familiar with operation of the diagnostics, as some of those programs are required for the calibration and alignment procedures herein. The necessary operating instructions are summarized here.

This section contains preventive maintenance instructions, and calibration and alignment procedures for the ADS and CRT, that are required with the diagnostics. A description of the built-in ODT debugging functions that can be used with the diagnostics is also included.

4.1 PREVENTIVE MAINTENANCE

This paragraph contains the preventative maintenance schedules for the 2511/2514 based on 40 hours per week operation - adjust schedules as appropriate for heavier usage.

	Monthly	Quarterly	Semi-Annually
Clean Box Filters		X	
Run CPU Diagnostics		X	
Check & Adjust Power Supplies		X	
Calibrate Analog Front End		X	
(A/D Input, Channel & Trigger Calibrations)			
Check & Adjust CRT			X
Verify Keyboard Functions		X	
Run Floppy Diagnostics		X	
Run Verify Diagnostic Program*	X		
Verify Optional Printer Operation		X	

*The verify program should be run each time the 2511/2514 system is assembled, disassembled or moved.

Cleaning. Turn all power off before cleaning the 2511/2514 systems. For access to the air filter, remove the six screws at the rear that attach the inner chassis to the outer cabinet rear bezel. (These are the inner rows of screws. Do not remove the outer six screws that attach the bezel to the cabinet.) Slide the chassis forward a few inches and peel the filter off from the ends. Knock off any dirt or dust that is large enough to fall free by its own weight and place the filter into a sink with warm, soapy water. Squeeze the suds through the filter several times until it is clean. Rinse well and squeeze out as much moisture as you can with a stack of paper towels, make sure that the filters are dry before replacing.

The exterior of the 2511/2514 may be cleaned with a mild detergent solution on a rag. Be sure the rag is just slightly moist. Be especially in the area of keys to be sure moisture does not "wick" in between the keys.

CAUTION

Never clean the system with solvents such as acetone or methylethylketone. These solvents may damage the paint or the plastic panel windows of the 2511/2514.

4.2 ADS CALIBRATION

The ADS calibration procedures (i.e., A/D, input channel and trigger level calibrations) are a subset of the 2511-0691 diagnostic package which must be performed before the RCT or the remainder of the 2511/2514 systems diagnostic manual is run.

NOTE

The remainder of the diagnostic routines must be run in the order in which they appear in the 2511/2514 systems Diagnostic Manual, Form 2511-0190.

4.2.1 Equipment Required

The following or equivalent equipment is required:

Nomenclature	Manufacturer	Model
Precision DC Voltage Source	Dial-A-Source	DAS46A
Digital Voltmeter	Dana	4300
Oscilloscope	Philip	PM3260E
Sine Wave Oscillator	GenRad	1309
Non-metallic Alignment Tool		
Circuit Board Extender Cards		

4.2.2 Software Required

Diagnostic disk 2511-0690	DYDP+
Diagnostic disk 2511-0691	RT-11

4.2.3 Power Supply Checks and Adjustments

Power supply checks are to be made at the ADS backplane, bottom rear. To gain access to the backplane, remove the chassis from the cabinet, turn it onto its side and remove the bottom of the box. If adjustments are necessary, they made at the rear of the power supply. To gain access to the rear of the power supply remove the power module from the back wall of the system box.

WARNING

Dangerous high voltages exist in this area. Disconnect ac power while removing the power module. For adjustments use a non-metallic alignment tool, do not disturb protective cover over terminal board, and be careful to avoid contact with ac power wiring.

Step 1. At the bottom rear of the ADS backplane, connect the negative lead of the DVM to E4 (Blue wire) for all of the following checks.

Step 2. Connect the positive lead of the DVM to the stud where the yellow wire is attached and adjust V1 for a voltage of +5 volts ±50 mV.

Step 3. Connect the positive lead of the DVM to E3 (purple and white wire) and adjust V3 for a voltage of +15 volts ±50 mV.

Step 4. Connect the positive lead of the DVM to E2 (gray and white wire) and adjust V4 for a voltage of -15 volts ±50 mV.

Step 5. Connect the positive lead of the DVM to E1 (red wire) and adjust V5 for a voltage of +12 volts ±50 mV.

4.2.4 Analog to Digital Calibration (Sample and A/D Board 2501-4711)

NOTE

The A/D, input channel, and trigger level calibration procedures must be performed as a group in the order which they are presented.

Step 1. Turn the main power switch at the front of the system box on and allow the system to warm up for ten minutes.

Step 2. Turn the main power switch on the front of the system box OFF.

Step 3. Remove the analog input and filter board (1923-4981) from slot six of the ADS backplane (closest to 2501-4713 board).

Step 4. Put the sample-hold, A/D mux board (2501-4711) on an extender.

Step 5. Connect the positive lead of the voltage source input to TP1 and ground to ~~TP31~~ TP32 (board 2501-4711).

Step 6. Mount diagnostic disk 2511-0691 on disk drive DY0.

Step 7. Turn the main power switch at the front of the system box ON. The system should boot, execute a startup file, and RUN TSD25A, the version of TSL used for diagnostics. If it does not, enter the RT-11 command **R TSD25A** to get the TSL/TSD prompting pointer (>).

Step 8. Load the ADS alignment program file: **>LOAD 'ADSAL1'(CR)**

Step 9. Run the A/D calibration routine: **>ADCAL 'A'(CR)**

Step 10. Press the **T** key to start the CRT printout.

NOTE

To stop the CRT printout press the **N** Key.

Step 11. Set the voltage source to -4.985 volts.

Step 12. Adjust R52 (offset pot 2501-4711 board) for an indication on the display of -.996 ±.003 (numerical value) or -4.985V ±.015V (volts).

Step 13. Set the voltage source to +4.985 volts.

Step 14. Adjust R53 (gain pot 2501-4711 board) for an indication of +.996 ±.003 or +4.985V ±.015V.

NOTE

The adjustments of R52 and R53 affect one another, so check and repeat steps 10-14 as necessary until both are within tolerance.

Step 15. Set the voltage source to 0 volts and verify a printout of 0 ±.002441 or 0 ±.0122 volts on the CRT. If the voltage is out of tolerance, repeat steps 9-14 until the displayed value of step 14 is within tolerance.

Step 16. Press the **S** key to stop the program.

Step 17. Turn off power and reinstall channel 'A' filterboard (1923-4981).

Step 18. Remove the board extender and voltage source input from the sample-hold, A/D and mux board (2501-4711).

Step 19. Calibrate the input channels as described in the next paragraph.

4.2.5 Input Channel(s) Calibration (Amplifier and Filter Board 1923-4981)

This procedure assumes that the A/D calibration routine has been completed and that the 'ADSAL1' programs are still loaded in memory. If ADSAL1 is not loaded in memory, perform steps 2, 6, 7, 8 of the A/D calibration above.

Step 1. Run the channel calibration routine as follows, where 'X' is the number of the channel to be calibration: **>CHCAL 'X'(CR)**

Step 2. Connect the positive lead of the DVM to TP2 on board 1923-4981 and the negative lead to TP7 (analog ground).

Step 3. Connect the voltage source to the channel under test using front BNC.

Step 4. Adjust the output of the voltage source to 0.0 volts.

Step 5. Adjust R5 (on board 1923-4981) until you get a reading of 0V ±10mV on the DVM.

Step 6. Set the voltage source output to +.1201 volts.

Step 7. Press the **G** Key.

Step 8. In response to the **?**, type in **.125(CR)**.

Step 9. Press the **T** Key to start the CRT printout.

NOTE

To stop the printout press the **N** Key.

Step 10. Adjust R8 (gain pot on board 1923-4981) for a reading of +.1201 ±.0006.

Step 11. Set the voltage source output to -.1201 volts and verify an output of -.1201 ±.0006.

Step 12. Press the **G** Key.

Step 13. In response to the ?, type in **2(CR)** (this sets the input range to 2 volts).

Step 14. Set the voltage source output to +1.800 volts.

Step 15. Adjust R2 (on board 1923-4981) for a reading of +1.800 ±.008.

Step 16. Set the voltage source output to -1.800 volts and verify an output of -1.800 ±.008 mV.

Step 17. Set the voltage source output to 0.0 volts.

Step 18. Press the **N** Key (this terminates the CRT display).

Step 19. Press the **G** Key.

Step 20. In response to the ?, type **.125(CR).** This sets the input range to .125 volts. The system should respond with a bell, indicating that automatic offset removal has been accomplished.

Step 21. Verify a voltage between -40 and +80 mV from the DVM at TP2.

Step 22. Repeat steps 19 through 21 for gains of .25, .5, 1, 2, 4, 8, and 16 to check all gain ranges.

Step 23. Press the **S** key to terminate the routine.

Step 24. Repeat steps 1 through 22 for all channels.

4.2.6 Trigger Level Calibration (Trigger Board 1923-4982)

This procedure assumes that the input channel(s) calibration routine has been completed and that the 'ADSAL1' programs are still loaded in memory. If ADSAL1 is not loaded in memory, perform steps 2, 6, 7, 8 of A/D calibration above.

Step 1. Connect the oscillator to the input connector of Channel 1 on the front of the box.

Step 2. Set the oscillator to output a 10 Hz sine wave, amplitude 4 volts peak to peak.

Step 3. Run the trigger calibration routine: **>TRGCAL(CR).** A sine wave should be displayed.

Step 4. Adjust R18 (trigger level control on board 1923-4982) so that the trigger point of the displayed sine wave is at 0 volts.

Step 5. Press the **S** Key to terminate the routine.

4.3 CRT ALIGNMENT

WARNING

Dangerous extremely high voltages are present in the CRT unit. Use extreme caution and non-metallic tools. If you are not familiar with TV service, refer to the manufacturing manual supplied with the system for additional precautions and general service information.

To gain access to the adjustment pots, loosen the two Phillips head screws on the rear of the cover and lift the cover off.

The calibration procedure is as follows:

Step 1. Mount the 2511-0691 diagnostic disk into DY0: and BOOT the system.

Step 2. When TSD/TSL starts (>), load the LIVE programs file: **>LOAD 'LIVE'(CR)**

Step 3. Run the GRID routine: **>GRID(CR).** A grid test pattern will be displayed on the CRT. If the grid test pattern displayed on the CRT matches the grid test pattern shown in Figure 4-1, proceed to Step 7. If not, proceed to step 4.

Step 4. Verify that the sides of the grid are parallel with the sides of the CRT. An example of a properly aligned grid test pattern is provided in Figure 4-2. If they are parallel proceed to Step 5. **(WARNING: High voltage area)** If they are not parallel, loosen the hex head screw (spintite) on the yoke clamp (tube neck) then rotate the yoke until the edges of the test pattern are parallel with the sides of the CRT and tighten the hexhead screw.

Step 5. Verify that the grid test pattern is centered on the CRT. If the test pattern is centered, proceed to Step 6. If not, adjust the centering rings (on the tube neck) until the test pattern is centered.

Step 6. Verify that the tops of the vertical test pattern lines are vertical. If they are vertical proceed to Step 7. If not, adjust horizontal hold R418 until they are vertical.

NOTE

The location of adjustment pots for this section is shown in Figure 4-1.

Step 7. Verify that the vertical component of the grid test is linear. If it is linear proceed to Step 8. If not, adjust R315 (vertical linearity) until it is linear.

Step 8. Run the CIRCLE routine: **>CIRCLE(CR).** A circle test pattern will be displayed on the CRT. An example of a properly aligned circle test pattern is provided in Figure 4-3. If the circle test pattern on the CRT matches that in Figure 4-3 proceed to Step 9. If it does not match, adjust L401 width coil and/or R312 (vertical size) for a true circular pattern on the CRT.

Step 9. The focus is adjusted at R429. Adjust as necessary.

Step 10. Press the **HALT** switch on the front of the system box.

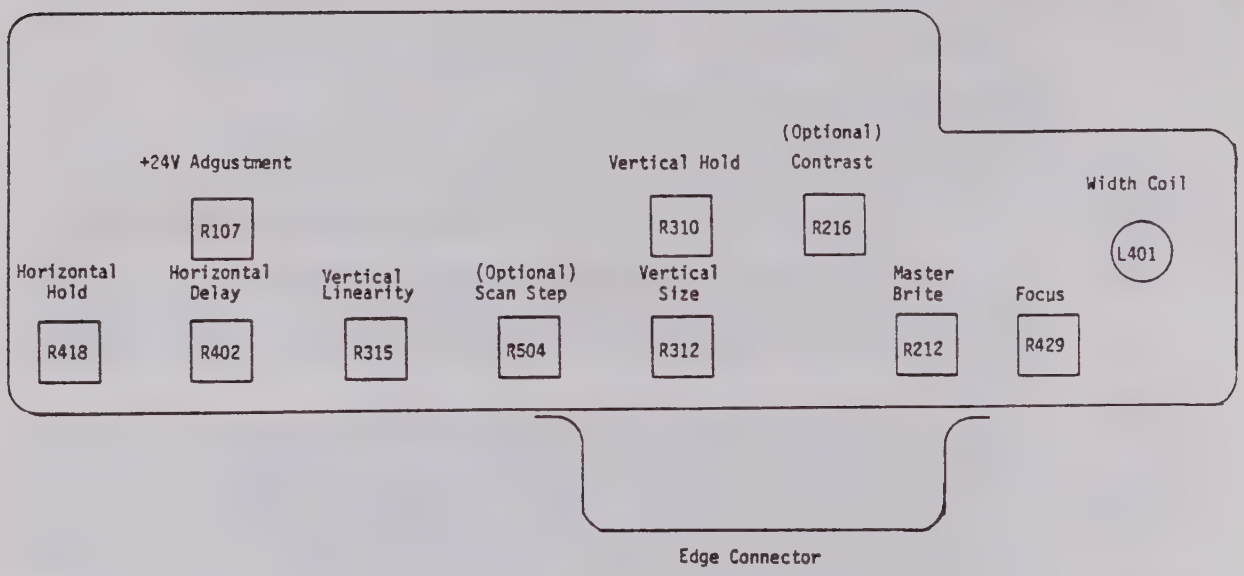


Figure 4-1. Calibration Pots

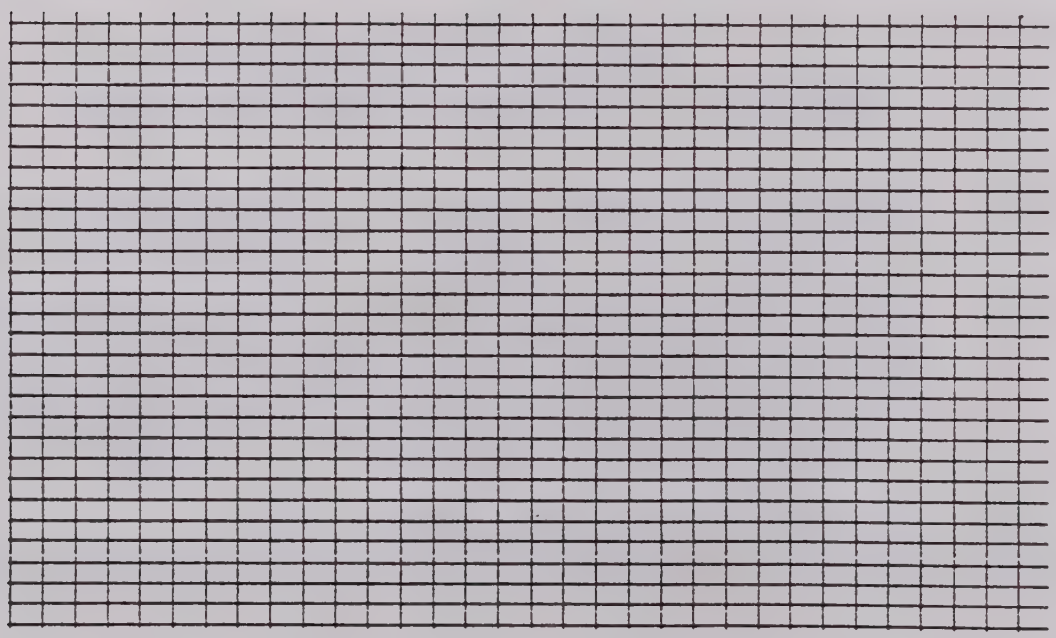


Figure 4-2. Properly Aligned GRID Test Pattern

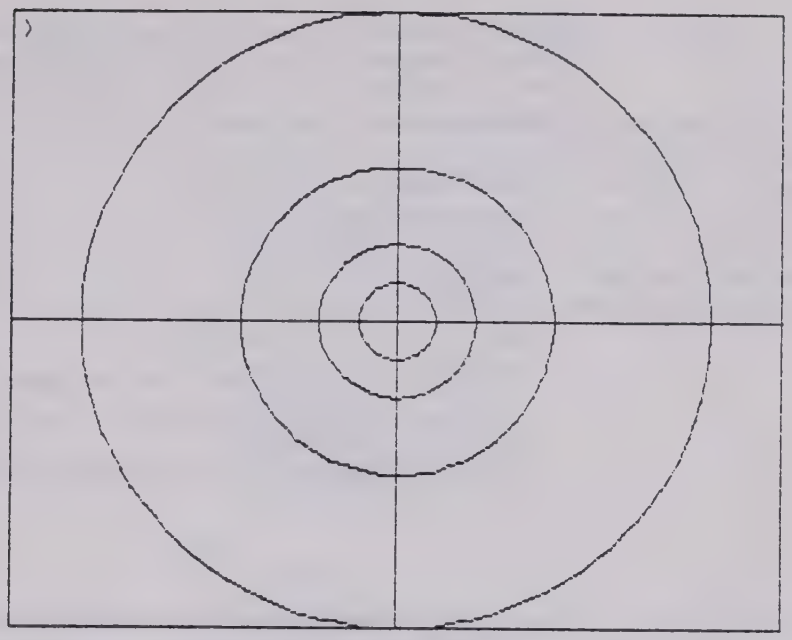


Figure 4-3. Properly Aligned CIRCLE Test Pattern

4.4 CONSOLE ODT DEBUGGING FUNCTIONS FOR THE LSI-11/2

Console ODT (Octal Debugging Tool) is a program in the LSI-11 microcode that provides for opening, examining, and modifying the content of registers and memory locations, and running or resuming programs from specified addresses. The system enters ODT when the processor HALTs, and displays an "at" sign (@) as the prompt for operator entries.

To specifically start ODT, press the front panel BOOT/HALT switch to HALT.

The following is a list of ODT commands and how they are used with the console terminal. Note that in the examples provided, operator entries are shown in bold face type. Only the commands necessary for implementing the required console functions are retained. Some output characters from the processor do not actually appear on the CRT, i.e., (LF). Regardless, they are still outputs.

All commands and characters are echoed by the processor. Illegal commands will be echoed followed by ?. This will be followed by (CR) (LF) and @. If a valid command character is received when no location is open (e.g., when having just entered the halt state), the valid command character will be echoed and followed by a ?(CR) (LF) @. Opening nonexistent locations will have the same response. The console always prints six numeric characters as addresses or data. However, the user is not required to type leading zeros for either address or data. If a bus error (timeout) occurs during memory refresh while in the console ODT mode, a (CR) (LF) @ will be typed. A list of the ODT commands and their uses follows:

COMMAND	SYMBOL	USE
Slash	/	This command is used to open a memory location, general-purpose register, or the processor status word. The / command is normally preceded by a location identifier.

Example:

@ **001000/**021515

where:

@ = ODT prompt character.

001000 = octal location in address space to be opened.

/ = command to open and exhibit contents of location.

012525 = contents of octal location 1000.

NOTE

If / is used without a preceding location identifier, the address of the last opened location is used. This feature can be used to verify data just entered in a location.

Carriage Return	(CR)	This command is used to close an open location. If the contents of the open location are to be changed, (CR) should be preceded by the new value. If no change to the location is necessary, (CR) will not alter its contents.

Example:

@**001000/**12525 **(CR)**

@/012525

or

Example:

@**001000/**012525 **15126421 (CR)**

@/126421

where:

(CR) is used to close location 1000 in both examples. Note that in the second example, the contents of location 1000 were changed and that only the last 6 digits entered were placed in location 1000.

COMMAND	SYMBOL	USE
Line Feed	(LF)↓	Note that on the 2511/2514 keyboard, the DOWN-arrow key is used for the for LINE FEED. This command is used to close an open location or general purpose register (GPR). If entered after a location has been opened, it will close the open location or GPR and open location +2 or GPR +1. If the contents of the open location or GPR are to be modified, the new contents should precede the ↓ operator.

Example:

@**1000**/012525↓

001002/005252 ↓

where:

↓ is used to close location 1000 and open location 1002 If used on the Processor Status (PS), ↓ will modify the PS if new data has been typed and close it. If ↓ is used to advance beyond R7, the register name printed is meaningless, but the contents printed are those of R0.

Up Caret	^	Note that on the 2511/2514 keyboard, this character is produced by SHIFT 6, not by the UP-arrow in the special keypad. The ^ command is also used to close an open location or GPR. If entered after a location or GPR has been opened, it will close the open location or GPR and open location -2, or GPR -1. If the contents of the open location or GPR are to be modified, the new contents should precede the ^ operator.

Example:

@ **1000**/012525^

000776/010101

where:

^ is used to close location 1000 and open location 776.

If used on the PS, the ^ will modify the PS if new data has been typed and close it. IF ^ is used to decrement below R0, the register name printed is meaningless but the content is that of R7.

COMMAND	SYMBOL	USE
At Sign	@	Once a location has been opened, the @ command is used to close that location and open a second location, using the contents of the first location as an indirect address to the second location; that is, the contents of the first location point to the second location to be opened. The contents of the first location can be modified before the @ command is used. This command is useful for stack operations. Example: @ **1000**/000200 @ 000200/000137 where: @ is used to close location 1000 and open location 200. Note that the @ command may be used with either GPRs or memory contents. If used on the PS, the command will modify the PS if new data is typed, and close it. However, the last GPR or memory location contents will be used as a pointer.
Back-arrow or Underscore	_	Note that on the 2511/2514 keyboard this character is produced by the underscore (i.e., SHIFT/ hyphen, not by the LEFT-arrow in the special keypad. This command is used once a location has been opened. ODT interprets the contents of the currently open word as an address indexed by the program counter (PC) and opens the addressed location. This is useful for relative instructions where it is desired to determine the effective address. Example: @ **1000**/00200 _ 001202/002525 where: _ is used to close location 1000 and open location 1202 (sum of contents of location 1000 which is 200, 1000, and 2). Note that this command cannot be used if a GPR or the PS is the open location and, if attempted, the command will modify the GPR or PS if data has been typed, and close the GPR or PS. A (CR) (LF) @ will then be issued.

COMMAND	SYMBOL	USE
Internal Register Designator	Rn	R command, if followed by a register value 0-7 (n) will allow that specific GPR to be opened if followed by the /command. Example: @**Rn**/012345 where: R = register designator. n = octal register 0-7. 012345 = contents of GPR n. Note that the GPRs once opened, can be closed with either the (CR), ↓, ^, or @ commands. The _ will also close a GPR but will not perform the relative mode operation.
Processor Status Word	RS	By replacing "n" in the above example with the letter S, the processor status word (PSW) will be opened. Example: @**RS**/000200 where: R = GPR or PSW designator. S = specified PS register and differentiates it from GPR's. 000200 = eight bit contents of PS; bit 7 = 1, all other bits = 0. Note that the contents of the PS can be changed using the (CR) command, but bit 4 (the T bit) cannot be modified using any of the commands.

COMMAND	SYMBOL	USE
Go	G	The "G" (GO) command is used to start execution of a program at the memory location typed immediately before the "G". Example: @ **100 G** The LSI-11 PC(R7) will be loaded with 100, the PS is cleared, and execution will begin at that location. Immediately after echoing the "G", two null (000) characters are sent to the console terminal serial line unit (SLU) to act as fill characters in case the bus BINIT L signal clears the SLU. Before starting execution, a BUS INIT is issued for 10 μs idle time. Note that a semicolon character can be used to separate the address from the G. This is done for LSI-11 ODT compatibility. Since the console is a character-by-character processor, as soon as the "G" is typed, the command is processed and a RUBOUT cannot be issued to cancel the command. If the B HALT L line is asserted, execution does not take place and only the BUS INIT sequence is done. The machine returns to console mode and prints the PC followed by (CR) (LF) @.
Proceed	P	The "P" (Proceed) command is used to continue or resume execution at the location pointed to by the current contents of the PC(R7). Example: @**P** If the BHALT L line is asserted or BOOT/INIT switch is held in INIT, a single instruction will be executed. The machine will return to console mode. It will print the contents of the PC followed by a (CR), (LF), @. In this fashion, it is possible to single instruction step through a user program. However, since the BHALT L line has higher priority than device interrupts, device interrupts will not be recognized in the single step mode. The semicolon is accepted for LSI-11 ODT compatibility. If the semicolon character is received during any character sequence, the console ignores it.

COMMAND	SYMBOL	USE
Maintenance	M	The "M" (Maintenance) command is used for maintenance purposes and prints the contents of an internal CPU register. This data reflects how the machine got to the console mode.

Example:

@ **M** 00213

@

The console prints six characters and then returns to command mode by printing (CR) (LF) @. The last octal digit is the only number of significance and is encoded as follows. The value specified how the machine got to the console mode.

Last Octal Digital Value	Function
0 or 4	Halt instruction or BHALT L
1 or 5	Bus error occurred while getting device interrupt vector. This error probably indicates that the priority chain (BIAKI/O L signal) is broken in the system and that an open slot exists between modules. It could also indicate that a device asserting BIRQ L did not latch its request. Modules must be inserted in a contiguous fashion according to the priority daisy chain.
2 or 6	Bus error occurred while doing memory refresh.
3	Double bus error occurred (stack contains nonexistent address).
4	Reserved instruction trap occurred (nonexistent Micro-PD address occurred on internal CPU bus).
7	A combination of 1, 2, and 4, which implies that all three conditions occurred.

NOTE

In the above example, the last octal digit is a "3", which indicates a double bus error occurred.

The codes listed above are valid only when the console mode is entered, and the code is immediately displayed. This information is lost when a "G" command is issued. The code reflects what happened in the program since the last "G" command was issued.

4.5 CONSOLE ODT DEBUGGING FUNCTIONS FOR THE LSI-11/23

Console ODT (Octal Debugging Tool) is a program in the LSI-11/23 microcode that provides for opening, examining, and modifying the content of registers and memory locations, and running or resuming programs from specified addresses. The system enters ODT when the processor HALTs, and displays an "at" sign (@) as the prompt for operator entries.

To specifically start ODT, press the front panel BOOT/HALT switch to HALT.

The following is a list of ODT commands and how they are used with the console terminal. Note that in the examples provided, operator entries are shown in bold faced type. Only the commands necessary for implementing the required console functions are retained. Some output characters from the processor do not actually appear on the CRT, i.e., line feed (LF). Regardless, they are still outputs.

All commands and characters are echoed by the processor. Illegal commands are echoed followed by ?. This will be followed by (CR) (LF) and @. If a valid command character is received when no location is open (e.g., when having just entered the halt state), the valid command character will be echoed and followed by a ?(CR) (LF) @. Opening nonexistent locations will have the same response. The console always prints six numeric characters as addresses or data. However, the user is not required to type leading zeros for either addresses or data. If a bus error (timeout) occurs during memory refresh while in the console ODT mode, a (CR) (LF) @ is printed. A list of the ODT commands and their uses follows:

COMMAND	SYMBOL	USE
Slash	/	This command is used to open an LSI-11 bus address, processor register, or processor status word and is normally preceded by other characters which specify a location. In response to /, console ODT prints the contents of the location (i.e., six characters) and then a space (ASCII 40). After printing is complete, console ODT waits for either new data for that location or a valid close command. The space character is issued so that the location's contents and possible new contents entered by the user are legible on the terminal.

Example:

@ **001000**/012525(SPACE)

where:

@	=	Console ODT prompt character.
001000	=	Octal location in the LSI-11 bus address space desired by the user (leading zeros mare not required).
/	=	Command to open and print contents of location.
012525	=	Contents of octal location 1000.
SPACE	=	Space character generated by console ODT.

COMMAND	SYMBOL	USE

The / command can be used without a location specifier to verify the data just entered into a previously opened location. The / is recognized only if it is entered immedialely after a prompt character. A / issued immediately after the processor enters ODT mode causes a ?(CR)(LF) to be printed because a location has not been opened.

Example:

@ **1000**/012525(SPACE) **1234(CR)**(CR)(LF)
@ /001234(SPACE)

where:

first line = new data of 1234 entered into location 1000 and locations closed with (CR)

second line = a / was entered without a location specifier and the previous location was opened to reveal that the new contents were correctly entered into memory.

Carriage Return (CR) This command is used to close an open location. If the contents of the open location are to be changed, (CR) should be preceded by the new value. If no change to the location is necessary, (CR) will not alter its contents.

Example:

@ **001000**/12525 **(CR)**
@ /012525

or

Example:

@ **001000**/012525 **15126421 (CR)**
@ /126421

(CR) is used to close location 1000 in both examples. Note that in the second example, the contents of location 1000 were changed and that only the last 6 digits entered were placed in location 1000.

COMMAND	SYMBOL	USE
Line Feed	(LF)↓	This command is used to close an open location and then open the next contiguous location. LSI-11 bus addresses and processor registers are incremented by 2 and 1 respectively. If the PS is open when a (LF) is issued, it is closed and a (CR)(LF)@ is printed; no new location is opened. If the open location's contents are to be changed, the new data should precede the (LF). If no data is entered, the location is closed without being altered.

Example:

@ **R2/**123456(SPACE)(CR)(LF)
@ **R3/**054321(SPACE)

In this case, the user entered (LF) with no data preceding it. In response, console ODT closed R2 and then opened R3. When a user has the last register, R7, open, and issues (LF), console ODT opens the beginning register, R1. When the user has the last LSI-11 bus address open of a 32K word segment and issues (LF), console ODT opens the first location of that same segment. If the user wishes to cross the 32K word boundary, he must reenter the address for the desired 32K word segment (i.e., console ODT is module 32K word). This operation is the same as that found on all other PDP-11 consoles.

Example:

@ **R7/**000000(SPACE)(CR)(LF)
@ **R0/**123456(SPACE)

or

@ **577776/**000001(SPACE)(**LF**)(CR)(LF)
@ **477776/**125252(SPACE)

Unlike other commands, console ODT does not echo the (LF). Instead it prints (CR), then (LF) so that terminal printers operate properly. In order to make this easier to decode, console ODT does not echo ASC11 0, 2, or 10 but responds to these three characters with ?(CR)(LF)@.

COMMAND	SYMBOL	USE
Line Feed	(LF)↓	This command is used to close an open location and then open the next contiguous location. LSI-11 bus addresses and processor registers are incremented by 2 and 1 respectively. If the PS is open when a (LF) is issued, it is closed and a (CR)(LF)@ is printed; no new location is opened. If the open location's contents are to be changed, the new data should precede the (LF). If no data is entered, the location is closed without being altered.

Example:

@ **R2/**123456(SPACE)↓(CR)(LF)
@ **R3/**054321(SPACE)

In this case, the user entered (LF) with no data preceding it. In response, console ODT closed R2 and then opened R3. When a user has the last register, R7, open, and issues (LF), console ODT opens the beginning register, R1. When the user has the last LSI-11 bus address open of a 32K word segment and issues (LF), console ODT opens the first location of that same segment. If the user wishes to cross the 32K word boundary, he must reenter the address for the desired 32K word segment (i.e., console ODT is module 32K word). This operation is the same as that found on all other PDP-11 consoles.

Example:

@ **R7/**000000(SPACE)↓(CR)(LF)
@ **R0/**123456(SPACE)

or

@ **577776/**000001(SPACE)↓(CR)(LF)
@ **477776/**125252(SPACE)

Unlike other commands, console ODT does not echo the (LF). Instead it prints (CR), then (LF) so that terminal printers operate properly. In order to make this easier to decode, console ODT does not echo ASC11 0, 2, or 10 but responds to these three characters with ?(CR)(LF)@.

COMMAND	SYMBOL	USE
Internal Register Designator	R or S	Either character when followed by a register number, 0 to 7, or PS designator, S, will open that specific processor register. The $ character is recognized to be compatible with ODT-11. The R character was introduced for the convenience of one key stroke and because it is representative of what it does. Example: @ **$0**/000123(SPACE) or @ **R7**/000123(SPACE)↓ @ **R0**/054321(SPACE) If more than one character is typed (digit or S) after the R or $, console ODT uses the last character as the register designator. There is an exception, however: if the last three digits are 077 or 477, ODT interprets it to mean the PS rather than R7.
Processor Status Word	S	This designator is for opening the PS (processor status word) and must be employed after the user has entered an R or $ register designator. Example: @ **RS**/100377(SPACE)**0(CR)**(CR)(LF) @ /000010(SPACE) Note that trace bit (bit 4) of the PS cannot be modified by the user. This is done so that PDP-11 program debug utilities (e.g., ODT-11), which use the T bit for signal-stepping, are not accidentally harmed by the user. If the user issues a (LF) while the PS is open, the PS is closed and ODT prints a (CR)(LF) @. No new location is opened in this case.

COMMAND	SYMBOL	USE
Proceed	P	The "P" (Proceed) command is used to continue or resume execution at the location pointed to by the current contents of the PC(R7).

Example:

@ **P**

Program execution resumes at the address pointed to by R7. After the P is echoed, the console ODT state is left and the processor immediately enters the state to fetch the next instruction. If the BHALT L bus signal is asserted, it is recognized at the end of the instruction (during the service state) and the processor enters the console ODT state. Upon entry, the content of the PC (R7) is printed. In this fashion, a user can single-instruction step through a program and get a PC "trace" displayed on his terminal.

4.5.1 LSI 11/73 Specific ODT Functions

Control-ShiftS (ASCII 23) - Binary Dump

This command is used for manufacturing test purposes and is not a normal user command. It is intended to display a portion of memory more efficiently than the and <LF> commands do. The protocol is as follows:

1. After a prompt character, ODT receives a control-shift-S command and echoes it.

2. The host system at the other end of the serial line must send two 8-bit bytes which ODT will interpret as a starting address. These two bytes are not echoed. The first byte specifies starting address <15:08> and the second byte specifies starting address <07:00>. Bus address bits <21:16> are always forced to 0; the DUMP command is restricted to the first 32 K words of address space.

3. After the second address byte has been received, ODT outputs 10_8 bytes to the serial line, starting at the address previously specified. When the output is finished, ODT will print <CR>, <LF>, @.

   If a user accidentally enters this comand, it is recommended that, in order to exit from the command, two @ characters (ASCII 100) be entered as a starting address. After the binary dump, the user will get the prompt character @.

Reserved Command

An ASCII H (110) is reserved for future use by Digital. If it is accidentally typed, ODT will echo the H and print a prompt character rather than a ?, which is the invalid character response. No other operation is performed.

4.5.2 LSI 11/73 Address Specification

The KDJ11-A micro-ODT accepts 22-bit addresses, allowing it to access 4088 M bytes of memory, plus the 8 Kbyte I/O page. All I/O page addresses must be entered by users with a full 22 bits specified. For example, if a user wishes to open the RCSR of the serial-line unit (SLU), he/she must enter 17777560, not 177560.

Processor I/O Addresses

Certain processor and MMU registers have I/O addresses assigned to them for programming purposes. If referenced in ODT, the PS will respond to its bus address, 17777776. Processor registers R0 through R7 will not respond (i.e., timeout wil occur) to bus addresses 17777700 through 17777707 if referenced in ODT.

The MMU status registers and PAR/PDR pairs can be accessed from ODT by entering their bus address.

Example: @ 17777572/000001<SPACE>

In this case, memory management status register 0 is opened to show the memory management enable bit set.

The FP11 accumulators cannot be accessed from ODT. Only FP11 instructions can access these registers.

Stack Pointer Selection

Accessing kernel and user stack pointer registers is accomplished in the following way. Whenever R6 is referenced in ODT, it accesses the stack pointer specified by the S current mode bits (PS<15:14>). This is done for convenience. If a program operating in kernel mode (PS<15:14> = 00) is halted, and R6 is opened, the kernel stack pointer is accessed.

Similarly, if a program is operating in user mode (PS<15:14> = 11), the R6 command accesses the user stack pointer. If a different stack pointer is desired, PS<15:14> must be set by the user to the appropriate value, and then the R6 command can be used. If an operating program has been halted, the original value of PS<15:14> must be restored in order to continue execution.

Example: PS = 140000
@R6/123456<SPACE>

The user mode stack pointer has been opened.

```
@R6/140000<SPACE> 0 <CR> <CR> _ <LF>
@R6/123456<SPACE> <CR> <CR> _ <LF>
@R6/000000<SPACE> 140000 <CR> <CR> _ <LF>
@P
```

In this case, the kernel mode stack pointer was desired. The PS was opened and PS<15:14> was restored, and then the program was continued using the P command.

APPENDIX A

AMD 2901B MICROPROCESSOR
DATA SHEETS

Am2901B

Four-Bit Bipolar Microprocessor Slice

Advanced Micro Devices
Bipolar Microprocessor Circuits

FINAL DATA – IMPROVED SET-UP TIMES
August, 1979

DISTINCTIVE CHARACTERISTICS

- Plug-in replacement for Am2901 and Am2901A
- Up to 27% faster than Am2901A, up to 50% faster than 2901
- High reliability plastic and cerdip packages
- Available now

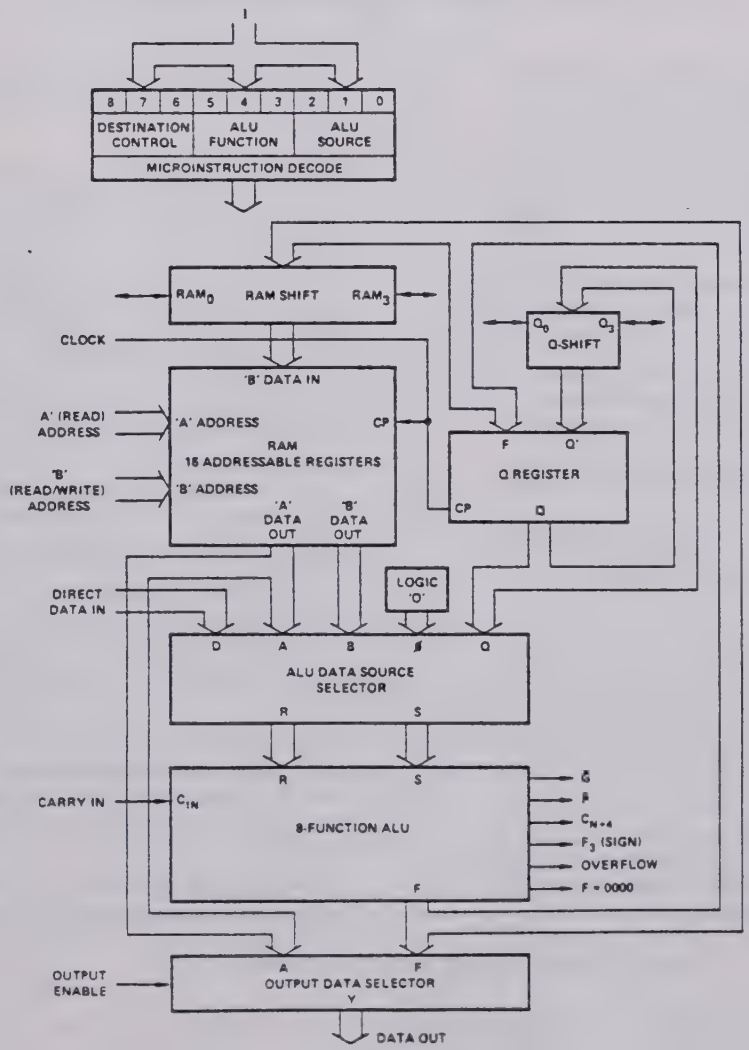
For applications information see the Am2900 Family Data Book and Chapters III and IV of "Build a Microcomputer", AMD's application series on the Am2900 family.

GENERAL DESCRIPTION

The four-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPU's, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the Am2901B will allow efficient emulation of almost any digital computing machine.

The device, as shown in the block diagram below, consists of a 16-word by 4-bit two-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The nine-bit microinstruction word is organized into three groups of three bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip. The Am2901B is a plug in replacement for the Am2901 or Am2901A.

MICROPROCESSOR SLICE BLOCK DIAGRAM



Mnemonic	MICRO CODE I_2	I_1	I_0	Octal Code	ALU SOURCE OPERANDS R	S
AQ	L	L	L	0	A	Q
AB	L	L	H	1	A	B
ZQ	L	H	L	2	0	Q
ZB	L	H	H	3	0	B
ZA	H	L	L	4	0	A
DA	H	L	H	5	D	A
DQ	H	H	L	6	D	Q
DZ	H	H	H	7	D	0

Figure 2. ALU Source Operand Control.

Mnemonic	MICRO CODE I_5	I_4	I_3	Octal Code	ALU Function	SYMBOL
ADD	L	L	L	0	R Plus S	R + S
SUBR	L	L	H	1	S Minus R	S − R
SUBS	L	H	L	2	R Minus S	R − S
OR	L	H	H	3	R OR S	$R \vee S$
AND	H	L	L	4	R AND S	$R \wedge S$
NOTRS	H	L	H	5	$\overline{R}$ AND S	$\overline{R} \wedge S$
EXOR	H	H	L	6	R EX-OR S	$R \veebar S$
EXNOR	H	H	H	7	R EX-NOR S	$\overline{R \veebar S}$

Figure 3. ALU Function Control.

Mnemonic	MICRO CODE I_8	I_7	I_6	Octal Code	RAM FUNCTION Shift	Load	Q-REG. FUNCTION Shift	Load	Y OUTPUT	RAM SHIFTER RAM_0	RAM_3	Q SHIFTER Q_0	Q_3
QREG	L	L	L	0	X	NONE	NONE	F → Q	F	X	X	X	X
NOP	L	L	H	1	X	NONE	X	NONE	F	X	X	X	X
RAMA	L	H	L	2	NONE	F → B	X	NONE	A	X	X	X	X
RAMF	L	H	H	3	NONE	F → B	X	NONE	F	X	X	X	X
RAMQD	H	L	L	4	DOWN	F/2 → B	DOWN	Q/2 → Q	F	F_0	IN_3	Q_0	IN_3
RAMD	H	L	H	5	DOWN	F/2 → B	X	NONE	F	F_0	IN_3	Q_0	X
RAMQU	H	H	L	6	UP	2F → B	UP	2Q → Q	F	IN_0	F_3	IN_0	Q_3
RAMU	H	H	H	7	UP	2F → B	X	NONE	F	IN_0	F_3	X	Q_3

X = Don't care. Electrically, the shift pin is a TTL input internally connected to a three-state output which is in the high-impedance state
B = Register Addressed by B inputs.
UP is toward MSB, DOWN is toward LSB.

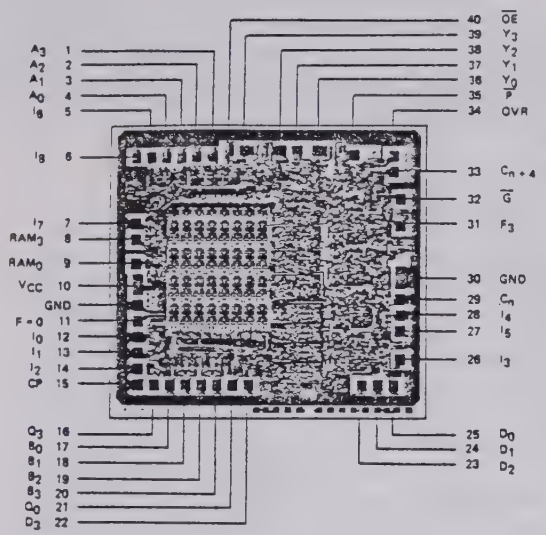
Figure 4. ALU Destination Control.

OCTAL I_{543}	OCTAL I_{210} 0	1	2	3	4	5	6	7
ALU Source / ALU Function	A, Q	A, B	0, Q	0, B	0, A	D, A	D, Q	D, 0
0 C_n = L R Plus S	A+Q	A+B	Q	B	A	D+A	D+Q	D
0 C_n = H R Plus S	A+Q+1	A+B+1	Q+1	B+1	A+1	D+A+1	D+Q+1	D+1
1 C_n = L S Minus R	Q−A−1	B−A−1	Q−1	B−1	A−1	A−D−1	Q−D−1	−D−1
1 C_n = H S Minus R	Q−A	B−A	Q	B	A	A−D	Q−D	−D
2 C_n = L R Minus S	A−Q−1	A−B−1	−Q−1	−B−1	−A−1	D−A−1	D−Q−1	D−1
2 C_n = H R Minus S	A−Q	A−B	−Q	−B	−A	D−A	D−Q	D
3 R OR S	$A \vee Q$	$A \vee B$	Q	B	A	$D \vee A$	$D \vee Q$	D
4 R AND S	$A \wedge Q$	$A \wedge B$	0	0	0	$D \wedge A$	$D \wedge Q$	0
5 $\overline{R}$ AND S	$\overline{A} \wedge Q$	$\overline{A} \wedge B$	Q	B	A	$\overline{D} \wedge A$	$\overline{D} \wedge Q$	0
6 R EX-OR S	$A \veebar Q$	$A \veebar B$	Q	B	A	$D \veebar A$	$D \veebar Q$	D
7 R EX-NOR S	$\overline{A \veebar Q}$	$\overline{A \veebar B}$	$\overline{Q}$	$\overline{B}$	$\overline{A}$	$\overline{D \veebar A}$	$\overline{D \veebar Q}$	$\overline{D}$

+ = Plus; − = Minus; $\vee$ = OR; $\wedge$ = AND; $\veebar$ = EX-OR

Figure 5. Source Operand and ALU Function Matrix.

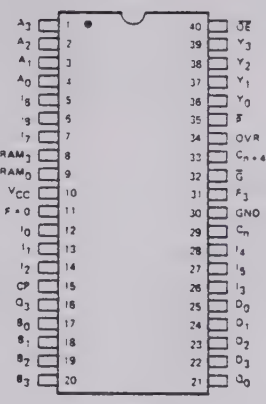
METALLIZATION AND PAD LAYOUT



DIE SIZE 0.117" X 0.128"

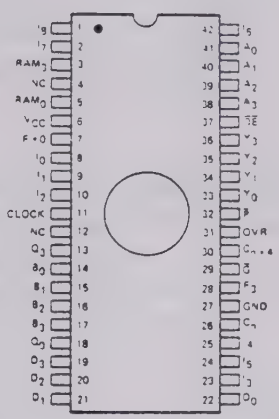
CONNECTION DIAGRAM
Top View

DIP



MPR-006

FLAT PACK CONNECTIONS
Top View



MPR-007

Note: Pin 1 is marked for orientation.

Figure 10.

PIN DEFINITIONS

A_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the A-port.

B_{0-3} The four address inputs to the register stack used to select one register whose contents are displayed through the B-port and into which new data can be written when the clock goes LOW.

I_{0-8} The nine instruction control lines. Used to determine what data sources will be applied to the ALU (I_{012}), what function the ALU will perform (I_{345}), and what data is to be deposited in the Q-register or the register stack (I_{678}).

Q_3 RAM_3 A shift line at the MSB of the Q register (Q_3) and the register stack (RAM_3). Electrically these lines are three-state outputs connected to TTL inputs internal to the device. When the destination code on I_{678} indicates an up shift (octal 6 or 7) the three-state outputs are enabled and the MSB of the Q register is available on the Q_3 pin and the MSB of the ALU output is available on the RAM_3 pin. Otherwise, the three-state outputs are OFF (high-impedance) and the pins are electrically LS-TTL inputs. When the destination code calls for a down shift, the pins are used as the data inputs to the MSB of the Q register (octal 4) and RAM (octal 4 or 5).

Q_0 RAM_0 Shift lines like Q_3 and RAM_3, but at the LSB of the Q-register and RAM. These pins are tied to the Q_3 and RAM_3 pins of the adjacent device to transfer data between devices for up and down shifts of the Q register and ALU data.

D_{0-3} Direct data inputs. A four-bit data field which may be selected as one of the ALU data sources for entering data into the device. D_0 is the LSB.

Y_{0-3} The four data outputs. These are three-state output lines. When enabled, they display either the four outputs of the ALU or the data on the A-port of the register stack, as determined by the destination code I_{678}.

$\overline{OE}$ Output Enable. When $\overline{OE}$ is HIGH, the Y outputs are OFF; when $\overline{OE}$ is LOW, the Y outputs are active (HIGH or LOW).

$\overline{G}$, $\overline{P}$ The carry generate and propagate outputs of the internal ALU. These signals are used with the Am2902 for carry-lookahead.

OVR Overflow. This pin is logically the Exclusive-OR of the carry-in and carry-out of the MSB of the ALU. At the most significant end of the word, this pin indicates that the result of an arithmetic two's complement operation has overflowed into the sign-bit.

F = 0 This is an open collector output which goes HIGH (OFF) if the data on the four ALU outputs F_{0-3} are all LOW. In positive logic, it indicates the result of an ALU operation is zero.

F_3 The most significant ALU output bit.

C_n The carry-in to the internal ALU.

C_{n+4} The carry-out of the internal ALU.

CP The clock input. The Q register and register stack outputs change on the clock LOW-to-HIGH transition. The clock LOW time is internally the write enable to the 16 x 4 RAM which compromises the "master" latches of the register stack. While the clock is LOW, the "slave" latches on the RAM outputs are closed, storing the data previously on the RAM outputs. This allows synchronous master-slave operation of the register stack.

PRELIMINARY DATA

ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (Unless Otherwise Noted)

(Group A, Subgroups 1, 2, and 3)

Parameters	Description	Test Conditions (Note 1)			Min	Typ (Note 2)	Max	Units
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}		I_{OH} = −1.6mA, Y_0, Y_1, Y_2, Y_3	2.4			Volts
				I_{OH} = −1.0mA, C_{n+4}	2.4			
				I_{OH} = −800µA, OVR, $\overline{P}$	2.4			
				I_{OH} = −600µA, F_3	2.4			
				I_{OH} = −600µA, $RAM_{0,3}$, $Q_{0,3}$	2.4			
				I_{OH} = −1.6mA, $\overline{G}$	2.4			
I_{CEX}	Output Leakage Current for F = 0 Output	V_{CC} = MIN., V_{OH} = 5.5V, V_{IN} = V_{IH} or V_{IL}					250	µA
V_{OL}	Output LOW Voltage	V_{CC} = MIN., V_{IN} = V_{IH} or V_{IL}	Y_0, Y_1, Y_2, Y_3	I_{OL} = 20mA (COM'L)			0.5	Volts
				I_{OL} = 16mA (MIL)			0.5	
			$\overline{G}$, F = 0	I_{OL} = 16mA			0.5	
			C_{n+4}	I_{OL} = 10mA			0.5	
			OVR, $\overline{P}$	I_{OL} = 8.0mA			0.5	
			F_3, $RAM_{0,3}$, $Q_{0,3}$	I_{OL} = 6.0mA			0.5	
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs (Note 7)			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs (Note 7)					0.8	Volts
V_I	Input Clamp Voltage	V_{CC} = MIN., I_{IN} = −18mA					−1.5	Volts
I_{IL}	Input LOW Current	V_{CC} = MAX., V_{IN} = 0.5V		Clock, $\overline{OE}$			−0.36	mA
				A_0, A_1, A_2, A_3			−0.36	
				B_0, B_1, B_2, B_3			−0.36	
				D_0, D_1, D_2, D_3			−0.72	
				I_0, I_1, I_2, I_6, I_8			−0.36	
				I_3, I_4, I_5, I_7			−0.72	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			−0.8	
				C_n			−3.6	
I_{IH}	Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.7V		Clock, $\overline{OE}$			20	µA
				A_0, A_1, A_2, A_3			20	
				B_0, B_1, B_2, B_3			20	
				D_0, D_1, D_2, D_3			40	
				I_0, I_1, I_2, I_6, I_8			20	
				I_3, I_4, I_5, I_7			40	
				$RAM_{0,3}$, $Q_{0,3}$ (Note 4)			100	
				C_n			200	
I_I	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{OZH} I_{OZL}	Off State (High Impedance) Output Current	V_{CC} = MAX.	Y_0, Y_1, Y_2, Y_3	V_O = 2.4V			50	µA
				V_O = 0.5V			−50	
			$RAM_{0,3}$ $Q_{0,3}$	V_O = 2.4V (Note 4)			100	
				V_O = 0.5V (Note 4)			−800	
I_{OS}	Output Short Circuit Current (Note 3)	V_{CC} = MAX. + 0.5V, V_O = 0.5V		$Y_0, Y_1, Y_2, Y_3, \overline{G}$	−30		−85	mA
				C_{n+4}	−30		−85	
				OVR, $\overline{P}$	−30		−85	
				F_3	−30		−85	
				$RAM_{0,3}$, $Q_{0,3}$	−30		−85	
I_{CC}	Power Supply Current (Note 6)	V_{CC} = MAX. (See Fig. 12)		T_A = 25°C		160	250	mA
			Am29018PC, DC	T_A = 0°C to +70°C			265	
				T_A = +70°C			220	
			Am29018DM, FM	T_C = −55°C to +125°C			265	
				T_C = +125°C			198	

Notes:
1. For conditions shown as MIN. or MAX., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
3. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
4. These are three-state outputs internally connected to TTL inputs. Input characteristics are measured with I_{678} in a state such that the three-state output is OFF.
5. "MIL" = Am2901BXM, DM, FM. "COM'L" = Am2901BXC, PC, DC.
6. Worst case I_{CC} is at minimum temperature.
7. These input levels provide zero noise immunity and should only be tested in a static, noise-free environment.

I. Am2901B Guaranteed Commercial Range Performance

The tables below specify the guaranteed performance of the Am2901B over the commercial operating range of 0°C to +70°C, with V_{CC} from 4.75V to 5.25V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BPC
Am2901BDC

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.)	69ns
Maximum Clock Frequency to shift Q (50% duty cycle, I = 432 or 632)	16MHz
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	69ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	60	61	59	50	70	67	71	–
D	38	36	40	33	48	44	45	–
Cn	30	29	23	–	37	29	38	–
I012	50	47	45	45	56	53	57	–
I345	49	48	44	45	54	49	53	–
I678	28	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	37	–	–	–	–	–	–	–
Clock ↓	49	48	47	37	58	55	59	29

C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	69 (Note 4)	0
B Destination Address	9	Do Not Change		0
D	–	–	51	0
Cn	–	–	39	0
I012	–	–	56	0
I345	–	–	55	0
I678	11	Do Not Change		0
RAM0, 3, Q0, 3	–	–	16	0

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	35	25

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

II. Am2901B Guaranteed Military Range Performance

The tables below specify the guaranteed performance of the Am2901B over the military operating range of −55°C to +125°C, with V_{CC} from 4.5V to 5.5V. All data are in ns, with inputs switching between 0V and 3V at 1V/ns and measurements made at 1.5V. All outputs have maximum DC load.

This data applies to the following part numbers: Am2901BDM
Am2901BFM

A. Cycle Time and Clock Characteristics.

Read-Modify-Write Cycle (from selection of A, B registers to end of cycle.	88ns
Maximum Clock Frequency to shift Q (50% duty cycle. I = 432 or 632)	15M
Minimum Clock LOW Time	30ns
Minimum Clock HIGH Time	30ns
Minimum Clock Period	88ns

B. Combinational Propagation Delays.
C_L = 50pF

To Output / From Input	Y	F3	Cn+4	$\overline{G}$, $\overline{P}$	F=0	OVR	RAM0 RAM3	Q0 Q3
A, B Address	82	84	80	70	90	86	94	–
D	44	38	40	34	50	45	48	–
Cn	34	32	24	–	38	31	39	–
I012	53	50	47	46	59	55	58	–
I345	53	50	46	45	58	50	55	–
I678	29	–	–	–	–	–	27	27
A Bypass ALU (I = 2XX)	50	–	–	–	–	–	–	–
Clock ↓	53	50	49	41	63	58	61	31

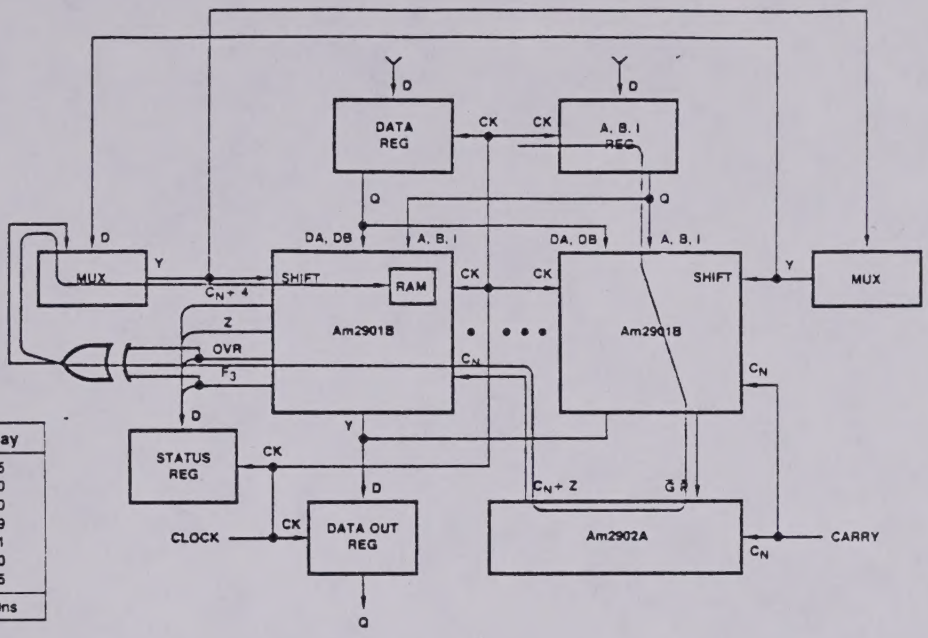
C. Set-up and Hold Times Relative to Clock (CP) Input.

Input	CP: Set-up Time Before H → L	Hold Time After H → L	Set-up Time Before L → H	Hold Time After L → H
A, B Source Address	20	0 (Note 3)	88 (Note 4)	0
B Destination Address	9	Do Not Change		0
D	–	–	55	0
Cn	–	–	42	0
I012	–	–	58	0
I345	–	–	58	0
I678	14	Do Not Change		0
RAM0, 3, Q0, 3	–	–	18	3

D. Output Enable/Disable Times.
Output disable tests performed with C_L = 5pF and measured to 0.5V change of output voltage level.

Input	Output	Enable	Disable
$\overline{OE}$	Y	40	35

Notes:
1. A dash indicates a propagation delay path or set-up time constraint does not exist.
2. Certain signals must be stable during the entire clock LOW time to avoid erroneous operation. This is indicated by the phrase "do not change".
3. Source addresses must be stable prior to the clock H → L transition to allow time to access the source data before the latches close. The A address may then be changed. The B address could be changed if it is not a destination; i.e. if data is not being written back into the RAM. **Normally A and B are not changed during the clock LOW time.**
4. The set-up time prior to the clock L → H transition is to allow time for data to be accessed, passed through the ALU, and returned to the RAM. It includes **all** the time from stable A and B addresses to the clock L → H transition, regardless of when the clock H → L transition occurs.

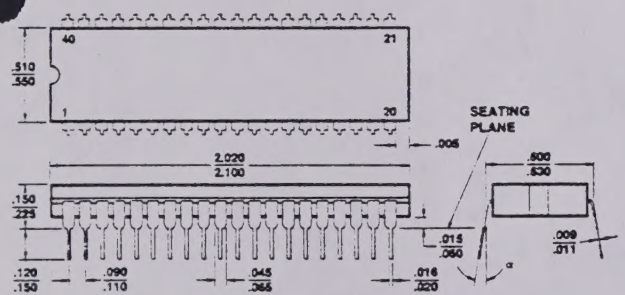


Device	Path	Delay
Register	C_D to Q	15
2901B	A, B to $\overline{G}$, $\overline{P}$	50
2902A	$\overline{G}$, $\overline{P}$ to C_{n+z}	10
2901B	C_n to F_3, OVR	29
XOR gate	in to out	11
Mux	D to Y	10
2901B	RAM_3 set-up	15
Total		140ns

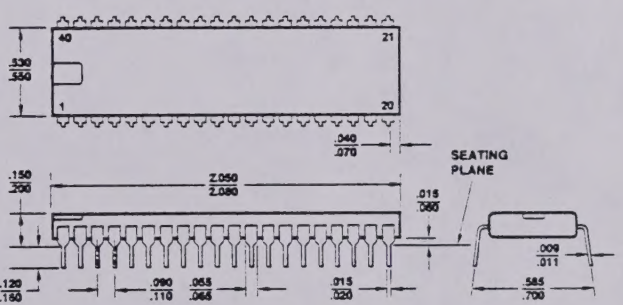
Example of speed calculation for two's complement arithmetic operation with shift down. The worst case speed path is shown in half-tone. For more detailed timing analysis, see Chapter III of "Build a Microcomputer," AMD's application series on the 2900 family.

PACKAGE OUTLINES

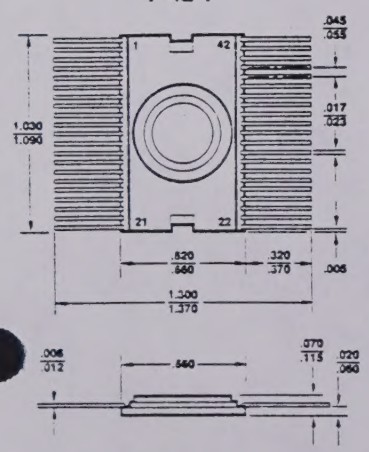
Cerdip
D-40-1



Molded
P-40-1



Flatpack
F-42-1



ORDERING INFORMATION

Order Number	Package Type (Note 1)	Operating Range (Note 2)	Screening Level (Note 3)
AM2901BPC	P-40	C	C-1
AM2901BDC	D-40	C	C-1
AM2901BDC-B	D-40	C	B-1
AM2901BDM	D-40	M	C-3
AM2901BDM-B	D-40	M	B-3
AM2901BFM	F-42	M	C-3
AM2901BFM-B	F-42	M	B-3
AM2901BXC	Dice	C	Visual inspection to MIL-STD-883 Method 2010B.
AM2901BXM	Dice	M	

Notes:
1. P = Molded DIP, D = Hermetic DIP, F = Flat Pak. Number following letter is number of leads. See Appendix B for detailed outline. Where Appendix B contains several dash numbers, any of the variations of the package may be used unless otherwise specified.
2. C = 0 to 70°C, V_{CC} = 4.75 to 5.25V; M = −55 to +125°C, V_{CC} = 4.50 to 5.50V
3. See Appendix A for details of screening. Levels C-1 and C-3 conform to MIL-STD-883, Class C. Level B-3 conforms to MIL-STD-883, Class B.

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